DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F9801

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F9801 is a μPD789800 subseries product (for a USB keyboard (for a PC)) of the 78K/0S series.

The μPD78F9801 replaces the internal masked ROM of the μPD789800 with flash memory, which enables the writing/erasing of a program while the device is mounted on the board.

Because the device can be programmed by the user, it is ideally suited to the evaluation stages of system development, the manufacture of small batches of multiple products, and the rapid development of new products.

The functions of this microcontroller are described in the following user's manuals. Refer to these manuals when designing a system based on this microcontroller.

μPD789800 Subseries User's Manual : U12978E
78K/0S Series User's Manual - Instruction : U11047E

FEATURES

- Pin-compatible with masked ROM version (excluding V_{PP} pin)
- Flash memory: 16K bytes
- Internal high-speed RAM: 256 bytes
- Operable on the same supply voltage as masked ROM version (V_{DD} = 4.0 to 5.5 V)

Remark The differences between the flash memory and masked ROM versions are summarized in **Chapter 3**.

APPLICATIONS

USB keyboards

★ ORDERING INFORMATION

Part Number	Package
μPD78F9801GB-8ES	44-pin plastic QFP (10 × 10 mm)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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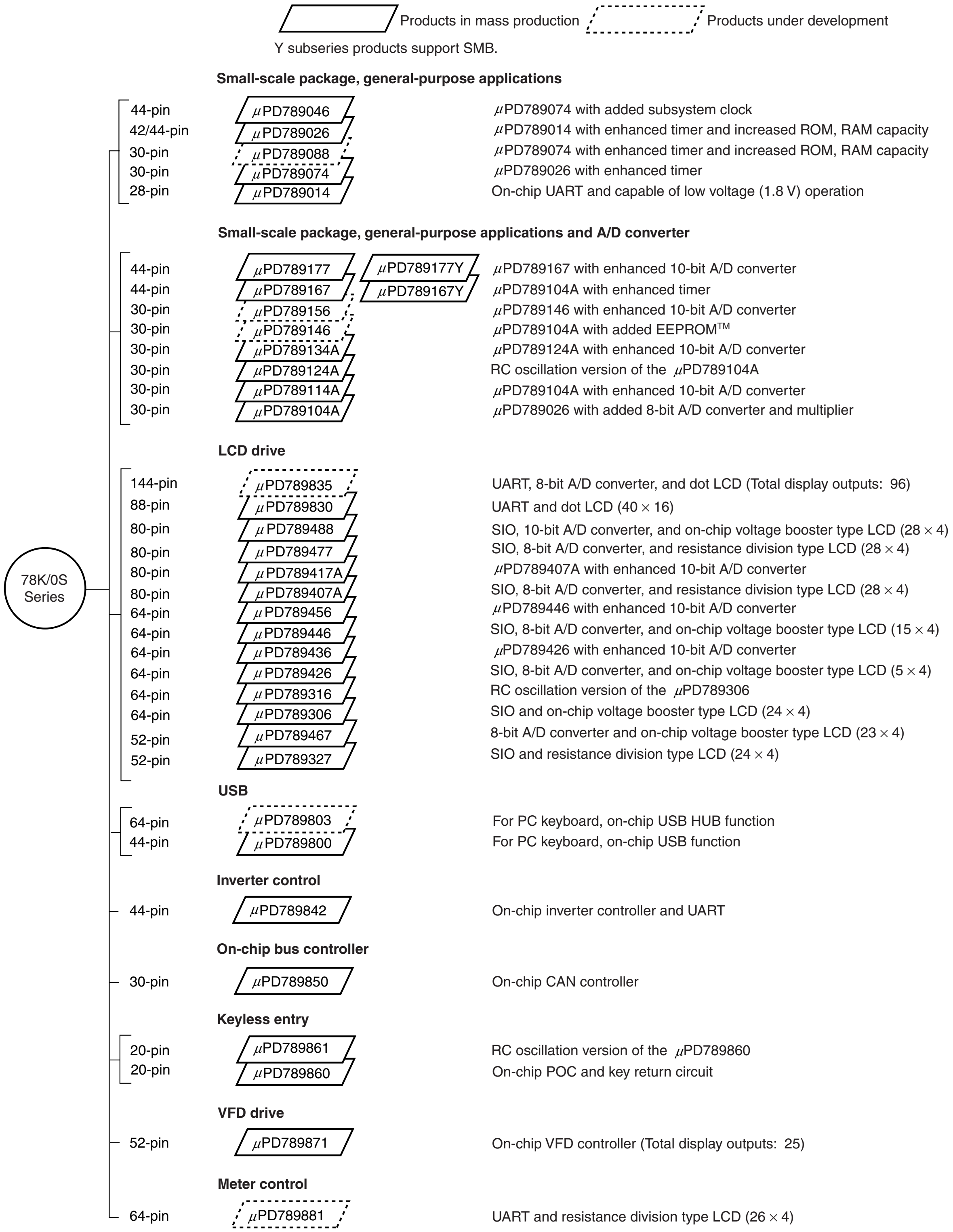
The mark ★ shows major revised points.

★ 78K/0S SERIES DEVELOPMENT

The 78K/0S series products are shown below. The sub-series names are indicated in frames.



Remark The vacuum fluorescent display (VFD) is a typical name. In some documents, however, it is described as the fluorescent indicator panel (FIP™). The VFD and FIP have identical functions.

The major functional differences among the subseries are listed below.

Series for General-Purpose Applications and LCD Drive

Subseries Name (Function →)		ROM Capacity (Bytes)	Timer 8-Bit	Timer 16-Bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remark
Small scale, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789088	16 K to 32 K	3 ch							24		
	μPD789074	2 K to 8 K	1 ch									
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale, general-purpose applications + A/D function	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch	1ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	37	1.8 V[Note]	Dot LCD support
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
	μPD789488	32 K	3 ch					8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789477	24 K					8 ch	–				
	μPD789417A	12 K to 24 K					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
	μPD789467	4 K to 24 K		–			1 ch		–	18		
	μPD789327						–		1 ch	21		

Note Flash memory version: 3.0 V

Series for ASSP

Subseries Name / Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remark
			8-Bit	16-Bit	Watch	WDT						
USB	μPD789803	8 K to 16 K	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	41	3.6 V	–
	μPD789800	8 K								31	4.0 V	
Inverter control	μPD789842	8 K to 16 K	3 ch	Note 1	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
On-chip bus controller	μPD789850	16 K	1 ch	1 ch	–	1 ch	4 ch	–	2 ch (UART: 1 ch)	18	4.0 V	–
Keyless entry	μPD789861	4 K	2 ch	–	–	1 ch	–	–	–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
Meter control	μPD789881	16 K	2 ch	1 ch	–	1 ch	–	–	1 ch (UART: 1 ch)	28	2.7 V Note 2	

Notes 1. 10-bit timer: 1 channel

2. Flash memory version: 3.0 V

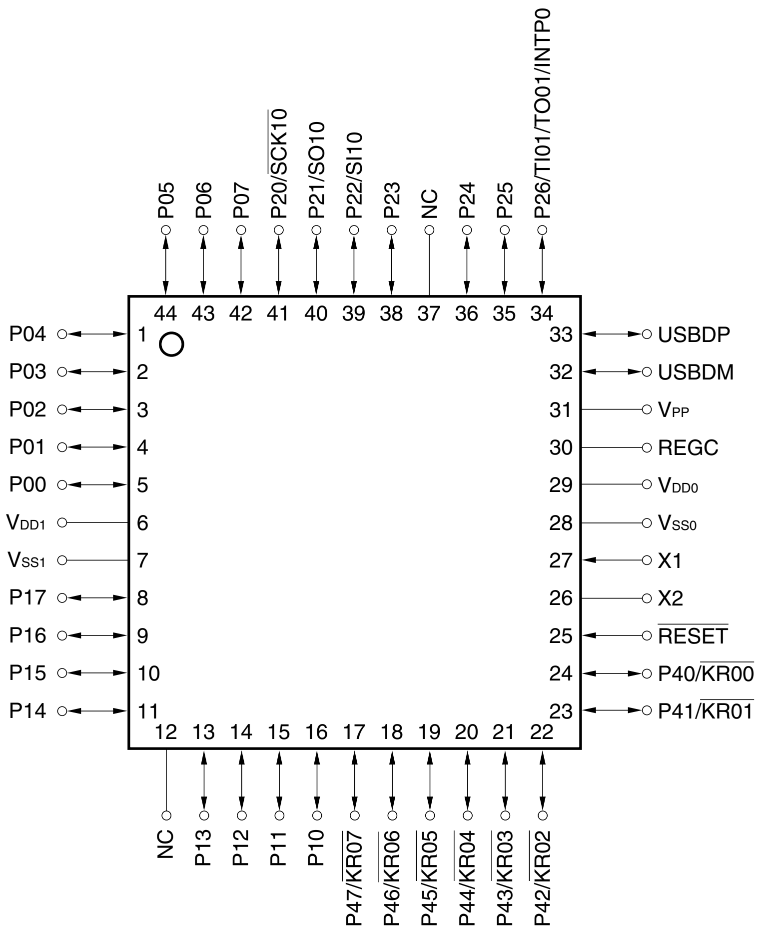
FUNCTIONS

Item		Function
Internal memory	Flash memory	16K bytes
	High-speed RAM	256 bytes
Minimum instruction execution time		0.33 μs/1.33 μs (when the system clock operates at 6.0 MHz)
General-purpose register		8 bits × 8 registers
Instruction set		• 16-bit operation • Bit manipulation (set, reset, and test) etc.
I/O ports		CMOS I/O: 31 pins (Of these, 18 pins can be switched to N-ch open-drain I/O pins.)
Serial interface		• USB (Universal Serial Bus) function : 1 channel • Three-wire serial I/O mode : 1 channel
Timer		• 8-bit timer 00 : 1 channel • 8-bit timer/event counter 01 : 1 channel • Watchdog timer : 1 channel
Regulator		Incorporated (V_{REG} = 3.3 ±0.3 V)
Vector interrupt source	Maskable	Internal: 9, external: 2
	Nonmaskable	Internal: 1
Power supply voltage		V_{DD} = 4.0 to 5.5 V
Operating ambient temperature		• T_A = -40 to +85 °C (when the USB is not operating) • T_A = 0 to +70 °C (when the USB is operating) • T_A = 10 to 40 °C (when a flash memory is written)
★ Package		44-pin plastic QFP (10 × 10 mm)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

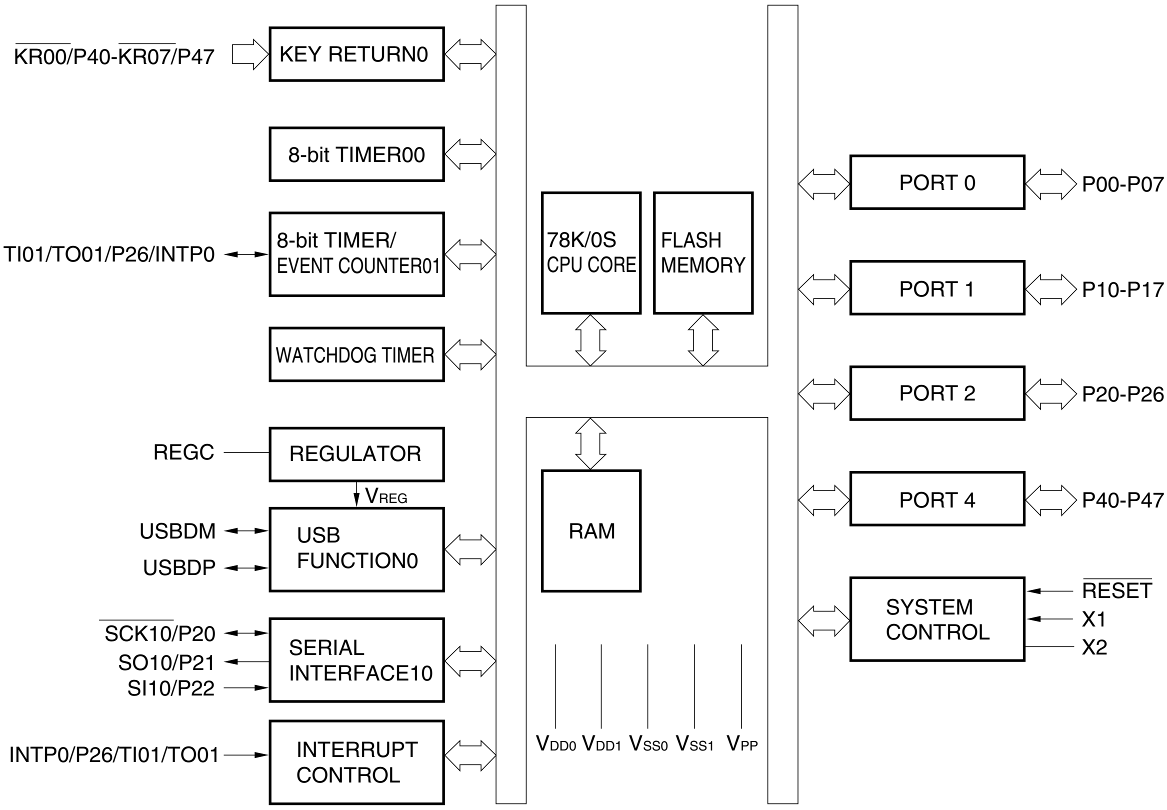
★ • 44-pin plastic QFP (10 x 10)
μPD78F9801GB-8ES



Caution In normal operation mode, connect the V_{PP} pin directly to the V_{SS0} or V_{SS1} pin.

INTP0	: Interrupt from peripherals	SI10	: Serial data input
$\overline{\text{KR00}}$ - $\overline{\text{KR07}}$	: Key return	SO10	: Serial data output
NC	: No connection	TI01	: Timer input
P00-P07	: Port 0	TO01	: Timer output
P10-P17	: Port 1	USBDM, USBDP	: Universal serial bus data
P20-P26	: Port 2	V_{DD0}, V_{DD1}	: Power supply
P40-P47	: Port 4	V_{PP}	: Programming power supply
$\overline{\text{RESET}}$	: Reset	V_{SS0}, V_{SS1}	: Ground
REGC	: Voltage regulator for USB function	X1, X2	: Crystal
$\overline{\text{SCK10}}$	: Serial clock input/output		

2. BLOCK DIAGRAM



3. DIFFERENCES BETWEEN μPD78F9801 AND MASKED ROM VERSION

The μPD78F9801 is a product that substitutes flash memory for the internal ROM of the masked ROM version (μPD789800). The differences between the μPD78F9801 and the masked ROM versions are shown in Table 3-1.

Table 3-1. Differences between μPD78F9801 and Masked ROM Version

Item		Flash Memory Version	Masked ROM Version
		μPD78F9801	μPD789800
Internal memory	ROM	16 Kbytes (Flash memory)	8 Kbytes
	High-speed RAM	256 bytes	
IC0 pin		Not provided	Provided
V_{PP} pin		Provided	Not provided
Electric characteristics		See the relevant data sheet.	

Caution There are differences in the amount of noise tolerance and noise radiation between flash memory versions and masked ROM versions. When considering changing from a flash memory version to a masked ROM version during process from experimental manufacturing to mass production, make sure to sufficiently evaluate the masked ROM versions using commercial samples (CS) (not engineering samples (ES)).

4. PIN FUNCTIONS

4.1 Port Pins

Pin Name	I/O	Function	When Reset	Also Used as
P00-P07	I/O	Port 0 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. CMOS output or N-ch open-drain output is specifiable in 8-bit units.	Input	-
P10-P17	I/O	Port 1 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. CMOS output or N-ch open-drain output is specifiable in 8-bit units.	Input	-
P20	I/O	Port 2 7-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. Only for P25 and P26, CMOS output or N-ch open-drain output is specifiable bit by bit.	Input	$\overline{\text{SCK10}}$
P21				SO10
P22				SI10
P23-P25				-
P26				INTP0/TI01/TO01
P40-P47	I/O	Port 4 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.	Input	$\overline{\text{KR00}}$ - $\overline{\text{KR07}}$

4.2 Non-Port Pins

Pin Name	I/O	Function	When Reset	Also Used as
INTP0	Input	External interrupt request input for which effective edges (rising and/or falling edges) can be specified	Input	P26/TI01/TO01
$\overline{\text{KR00}}$ - $\overline{\text{KR07}}$	Input	Input for detecting key return signals	Input	P40-P47
REGC	-	Internally generated power supply for driving USB driver/receiver. Connect this pin to V_{SS} through a 220-Ω resistor and a 0.1-μF capacitor.	-	-
$\overline{\text{RESET}}$	Input	System reset input	Input	-
$\overline{\text{SCK10}}$	I/O	Serial clock input/output for serial interface	Input	P20
SI10	Input	Serial data input for serial interface	Input	P22
SO10	Output	Serial data output for serial interface	Input	P21
TI01	Input	External count clock input to 8-bit timer/event counter 01	Input	P26/INTP0/TO01
TO01	Output	Timer output from 8-bit timer/event counter 01	Input	P26/INTP0/TI01
USBDM	I/O	Serial data input/output (negative side) for USB function. The pull-up resistor (1.5 kΩ) for the USBDM pin must be connected to the REGC pin.	Input	-
USBDP	I/O	Serial data input/output (positive side) for USB function	Input	-
X1	Input	Connected to crystal for system clock oscillator	Input	-
X2	-		-	
V_{DD0}	-	Positive supply voltage for ports	-	-
V_{DD1}	-	Positive supply voltage for circuits other than ports	-	-
V_{SS0}	-	Ground potential for ports	-	-
V_{SS1}	-	Ground potential for circuits other than ports	-	-
V_{PP}	-	Flash memory programming mode setting. High-voltage application for program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	-	-
NC	-	Not internally connected. Leave this pin open.	-	-

4.3 Pin Input/Output Circuits and Handling of Unused Pins

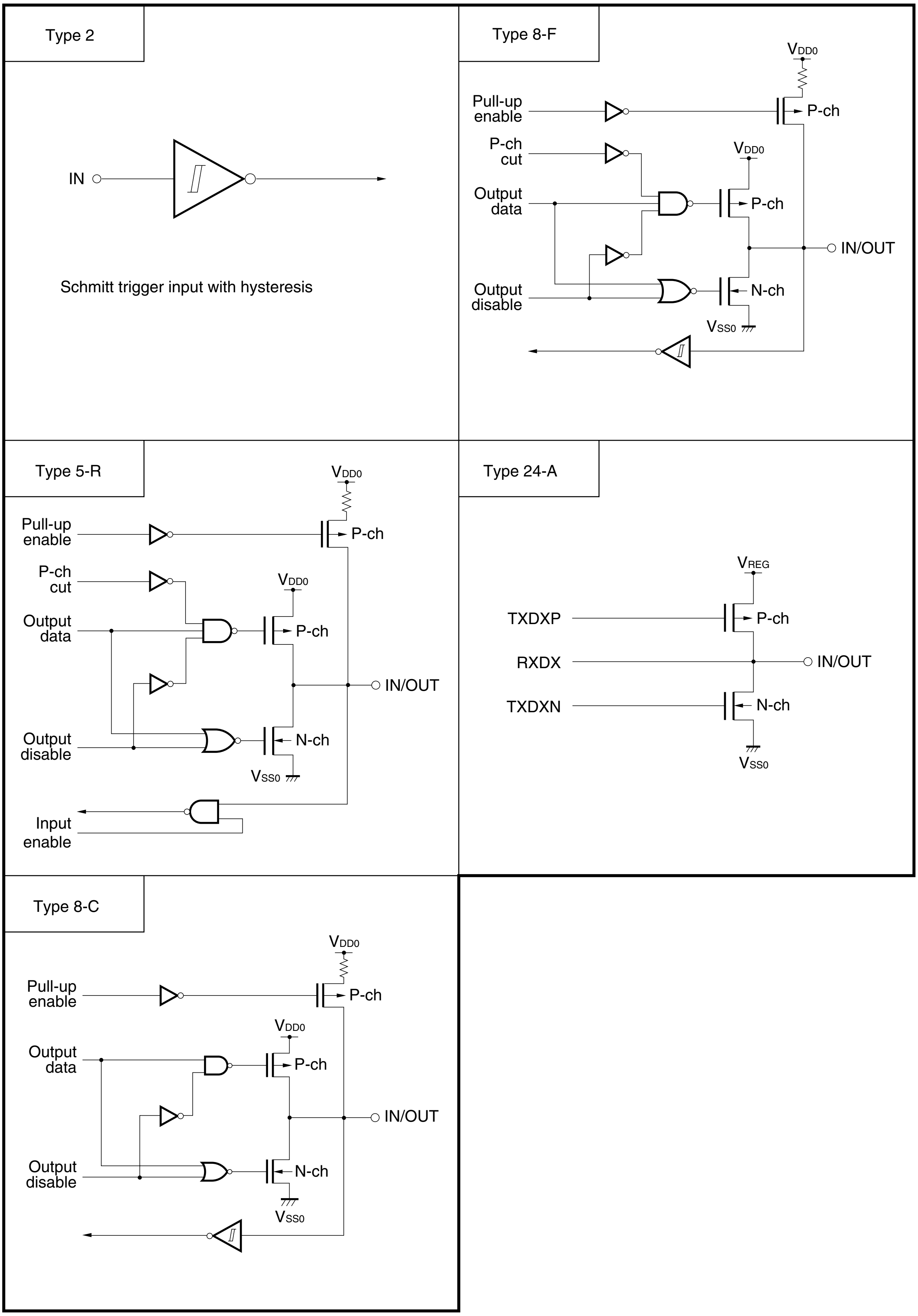
Table 4-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.

Figure 4-1 shows the configuration of each type of input/output circuit.

Table 4-1. Type of Input/Output Circuit for Each Pin

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00-P07	5-R	I/O	Input : Connect these pins separately to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via respective resistors. Output : Leave these pins open.
P10-P17			
P20/$\overline{SCK10}$	8-C		
P21/SO10			
P22/SI10			
P23, P24			
P25	8-F		
P26/INTP0/TI01/TO01			
P40/$\overline{KR00}$ -P47/$\overline{KR07}$	8-C		
USBDM	24-A		Connect this pin to the REGC pin.
USBDP			Connect this pin to V_{SS0} or V_{SS1} via resistors.
$\overline{RESET}$	2	Input	-
V_{PP}	-	-	Connect this pin directly to V_{SS0} or V_{SS1}.
NC	-	-	Leave this pin open.
REGC	-	-	Connect this pin to the USBDM pin.

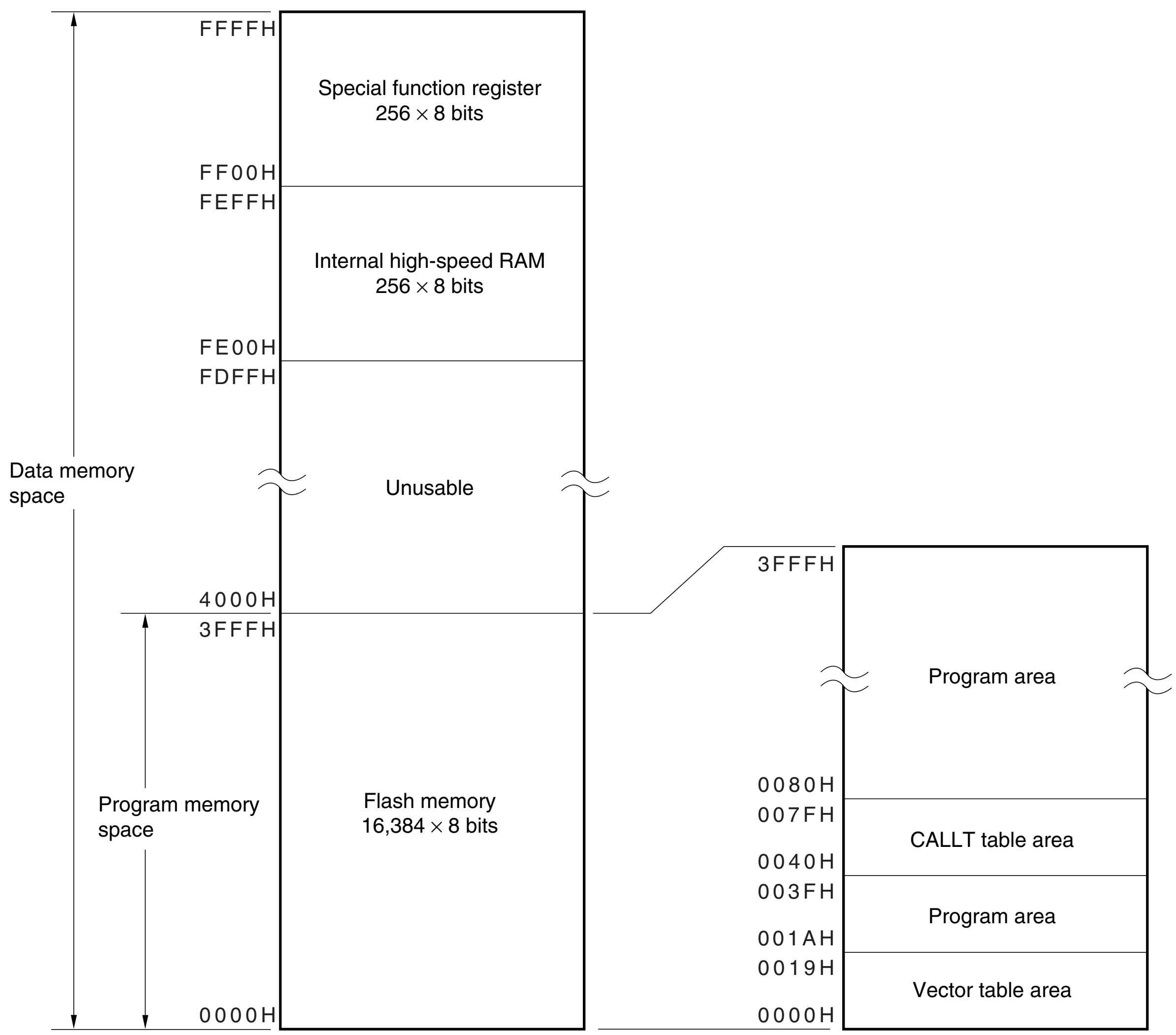
Figure 4-1. Pin Input/Output Circuits



5. MEMORY SPACE

Figure 5-1 shows the memory map of the μPD78F9801.

Figure 5-1. Memory Map



6. FLASH MEMORY PROGRAMMING

The on-chip program memory in the μPD78F9801 is a flash memory.

The flash memory can be written with the μPD78F9801 mounted on the target system (on-board). Connect the dedicated flash programmer (Flashpro III (model number: FL-PR3, PG-FP3)) to the host machine and target system to write to the flash memory.

Remark FL-PR3 is made by Naito Densei Machida Mfg. Co., Ltd.

6.1 Selecting Communication Mode

The flash memory is written by using Flashpro III and by means of serial communication. Select a communication mode from those listed in Table 6-1. To select a communication mode, the format shown in Figure 6-1 is used. Each communication mode is selected by the number of V_{PP} pulses shown in Table 6-1.

★ **Table 6-1. Communication Mode List**

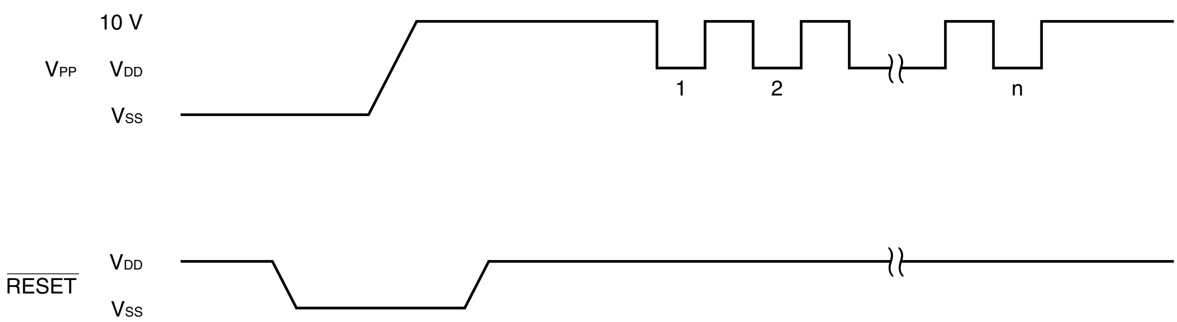
Communication Mode	Pins Used[Note 1]	Number of V_{PP} Pulses
3-wired serial I/O mode	$\overline{SCK10}$/P20 SO10/P21 SI10/P22	0
Pseudo 3-wire mode[Note 2]	P10 (Serial clock input) P11 (Serial data output) P12 (Serial data input)	12

Notes 1. When changed to flash programming mode, all pins unused for flash memory programming enter the same state as that immediately upon a reset. Therefore, when the external device connected to the port does not recognize the state of the port immediately upon a reset, connect these pins to the V_{DD} pin via a resistor or to the V_{SS0} or V_{SS1} pin via a resistor.

2. Serial transfer is performed by controlling a port by software.

Caution Be sure to select a communication mode depending on the V_{PP} pulse number shown in Table 6-1.

Figure 6-1. Communication Mode Selection Format



6.2 Function of Flash Memory Programming

By transmitting/receiving commands and data in the selected communication mode, operations such as writing to the flash memory are performed. Table 6-2 shows the major functions of flash memory programming.

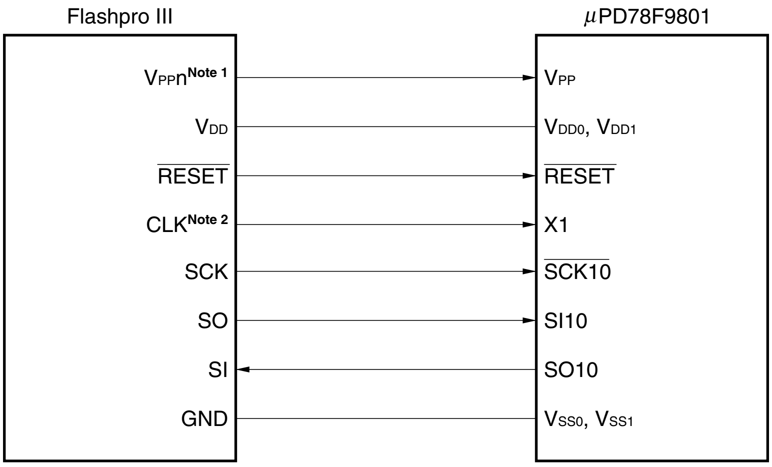
Table 6-2. Functions of Flash Memory Programming

Function	Description
Batch erase	Erases all contents of memory.
Batch blank check	Checks erased state of entire memory.
Data write	Writes to flash memory based on write start address and number of data written (number of bytes).
Batch verify	Compares all contents of memory with input data.

★ 6.3 Flashpro III Connection

How the Flashpro III is connected to the μPD78F9801 differs depending on the communication mode (3-wired serial I/O or pseudo 3-wire mode). Figures 6-2 and 6-3 show the connection in the respective mode.

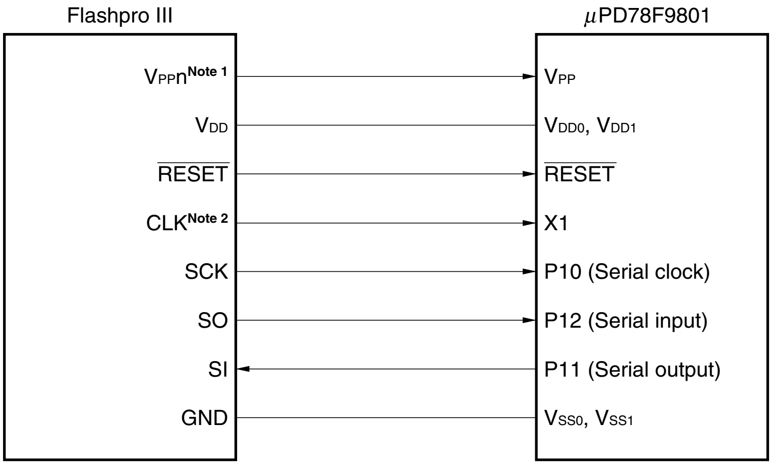
Figure 6-2. Flashpro III Connection in 3-Wired Serial I/O Mode



Notes 1. n = 1, 2

2. Connect the CLK pin when the system clock is input from the Flashpro III. When the resonator has already been connected to the X1 pin, there is no need to connect the CLK pin to the X1 pin.

Figure 6-3. Flashpro III Connection in Pseudo 3-Wire Mode



Notes 1. n = 1, 2

2. Connect the CLK pin when the system clock is input from the Flashpro III. When the resonator has already been connected to the X1 pin, there is no need to connect the CLK pin to the X1 pin.

6.4 Example of Settings for Flashpro III (PG-FP3)

Set as follows when writing to flash memory using the Flashpro III (PG-FP3).

<1> Download the parameter file.
<2> Select the serial mode and the serial clock using the type command.
<3> The following is a setting example using the PG-FP3.

★ **Table 6-3. Example Using PG-FP3**

Communication Mode	Setting Example Using PG-FP3		Number of V_{PP} Pulses[Note]
3-wired serial I/O mode	COMM PORT	SIO ch-0	0
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
Pseudo 3-wire mode	COMM PORT	Port A	12
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.1943 MHz	
	SIO CLK	1 kHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1 kHz	

Note The number of V_{PP} pulses supplied from the Flashpro III during serial communication initialization. The pins to be used in communication are determined by this number of pulses.

Remark COMM PORT : Selection of serial port
SIO CLK : Selection of serial clock frequency
CPU CLK : Selection of CPU clock source to be input

7. INSTRUCTION SET OVERVIEW

The instruction set for the μPD78F9801 is listed later.

7.1 Legend

7.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform with the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and a pair of [and] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [and]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or a pair of [and].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other parenthesized names listed in Table 7-1).

Table 7-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

7.1.2 Descriptions of the operation field

A	:	A register (8-bit accumulator)
X	:	X register
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
AX	:	AX register pair (16-bit accumulator)
BC	:	BC register pair
DE	:	DE register pair
HL	:	HL register pair
PC	:	Program counter
SP	:	Stack pointer
PSW	:	Program status word
CY	:	Carry flag
AC	:	Auxiliary carry flag
Z	:	Zero flag
IE	:	Interrupt request enable flag
NMIS	:	Flag to indicate that a nonmaskable interrupt is being handled
()	:	Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L	:	Upper and lower 8 bits of a 16-bit register
$\wedge$	:	Logical product (AND)
$\vee$	:	Logical sum (OR)
$\forall$	:	Exclusive OR
—	:	Inverted data
addr16	:	16-bit immediate data or label
jdisp8	:	Signed 8-bit data (displacement value)

7.1.3 Description of the flag operation field

(Blank)	:	No change
0	:	To be cleared to 0
1	:	To be set to 1
×	:	To be set or cleared according to the result
R	:	To be restored to the previous value

7.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except when r = A.
2. Except when r = A or X.
3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP − 1) ← $(PC + 3)_H$, (SP − 2) ← $(PC + 3)_L$, PC ← addr16, SP ← SP − 2			
CALLT	[addr5]	1	8	(SP − 1) ← $(PC + 1)_H$, (SP − 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1), PC_L ← (00000000, addr5), SP ← SP − 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP − 1) ← PSW, SP ← SP − 1			
	rp	1	4	(SP − 1) ← rp_H, (SP − 2) ← rp_L, SP ← SP − 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC_H ← A, PC_L ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

8. ELECTRICAL CHARACTERISTICS

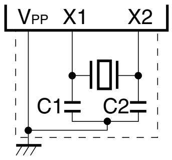
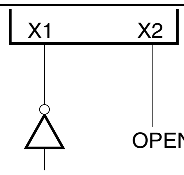
ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions	Rated Value	Unit
Supply voltage	V_{DD}		-0.3 to +6.5	V
	V_{PP}		-0.3 to +10.5	V
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V
Output high current	I_{OH}	Each pin	-10	mA
		Total for all pins	-30	mA
Output low current	I_{OL}	Each pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A	In normal operation mode	-40 to +85	°C
		During flash memory programming	10 to 40	°C
Storage temperature	T_{stg}		-40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.
That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

CHARACTERISTICS OF THE SYSTEM CLOCK OSCILLATION CIRCUIT
(T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillator frequency (f_X)Note 1		6.0	6.0	6.0	MHz
		Oscillation settling timeNote 2				10	ms
External clock		X1 input frequency (f_X)Note 1		6.0	6.0	6.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		71		83	ns

Notes 1. Only the characteristics of the oscillator are indicated. See the description of the AC characteristics for the instruction execution time.

2. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected. Use a resonator that can settle oscillation before the oscillation settling time expires.

Caution When using the system clock oscillator, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS0}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillator.**

FLASH MEMORY WRITE/DELETE CHARACTERISTICS (T_A = 10 to 40 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin)	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (in 6.0-MHz operation mode)			18Note	mA
Write current (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			7.5	mA
Delete current (V_{DD} pin)	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (in 6.0-MHz operation mode)			18Note	mA
Delete current (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			100	mA
Unit delete time	t_{er}		1	1	1	s
Total delete time	t_{era}				20	s
Write count		Delete/write are regarded as 1 cycle.			1	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		0.2V_{DD}	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

Note The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output high current	I_{OH}	Each pin				-1	mA
		Total for all pins				-15	mA
Output low current	I_{OL}	Each pin				10	mA
		Total for all pins				80	mA
Input high voltage	V_{IH1}	P00-P07, P10-P17		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20-P26, P40-P47		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	X1		V_{DD} - 0.1		V_{DD}	V
	V_{IH4}	USBDM, USBDP T_A = 0 to +70 °C		2.0		3.6	V
Input low voltage	V_{IL1}	P00-P07, P10-P17		0		$0.3V_{DD}$	V
	V_{IL2}	$\overline{\text{RESET}}$, P20, P22, P40-P47		0		$0.2V_{DD}$	V
	V_{IL3}	X1		0		0.1	V
	V_{IL4}	USBDM, USBDP T_A = 0 to +70 °C		0		0.8	V
Output high voltage	V_{OH1}	Pins other than USBDM and USBDP	I_O = -1 mA	V_{DD} - 1.0			V
	V_{OH2}	USBDM, USBDP T_A = 0 to +70 °C, RL = 15 kΩ (connected to V_{SS})[Note 1]		2.8			V
Output low voltage	V_{OL1}	Pins other than USBDM and USBDP	I_O = 10 mA			1.0	V
	V_{OL2}	USBDM, USBDP T_A = 0 to +70 °C, RL = 15 kΩ (connected to V_{DD})[Note 1]				0.3	V
High-level input leakage current	I_{LIH1}	Pins other than X1, X2, USBDM, and USBDP	$V_I = V_{DD}$			3	μA
	I_{LIH2}	X1, X2	$V_I = V_{DD}$			20	μA
	I_{LIH3}	USBDM, USBDP T_A = 0 to +70 °C	0 V ≤ V_I ≤ V_{REG}			10	μA
Low-level input leakage current	I_{LIL1}	Pins other than X1, X2, USBDM, and USBDP	V_I = 0 V			-3	μA
	I_{LIL2}	X1, X2	V_I = 0 V			-20	μA
	I_{LIL3}	USBDM, USBDP T_A = 0 to +70 °C	0 V ≤ V_I ≤ V_{REG}			-10	μA
High-level output leakage current	I_{LOH}	V_O = 0 V				3	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V				-3	μA
Software pull-up resistor	R	V_I = 0 V		50	100	200	kΩ
Regulator output voltage	V_{REG}	I_O = 0 to -3 mA		3.0	3.3	3.6	V
Supply current[Note 2]	I_{DD1}	6.0-MHz crystal oscillation (operating mode)[Note 3]			5.0	10.0	mA
	I_{DD2}	6.0-MHz crystal oscillation (HALT mode)[Note 3]			1.5	3.5	mA
	I_{DD3}	STOP mode	When the USB function is disabled		10	30	μA
			When the USB function is enabled (T_A = 0 to +70 °C)		50	100	μA

Notes 1. RL is a resistor connected to a bus line.

2. The power supply current does not include the current flowing through the on-chip pull-up resistor.

3. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H)

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

AC CHARACTERISTICS

(1) Basic operations (T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	When PCC = 00H (f_X = 6.0 MHz)	0.333	0.333	0.333	μs
		When PCC = 02H (f_X = 6.0 MHz)	1.333	1.333	1.333	μs
TI01 input frequency	f_{TI}		0		4.0	MHz
TI01 input high/low level width	t_{TIH}, t_{TIL}		0.1			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INTP0	10			μs
$\overline{\text{RESET}}$ input low level width	t_{RSL}		10			μs

(2) Serial interface

(a) USB function (T_A = 0 to +70 °C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USBDM and USBDP rise time	t_R	CL = 50 pF Note	75			ns
		CL = 350 pF Note			300	ns
USBDM and USBDP fall time	t_F	CL = 50 pF Note	75			ns
		CL = 350 pF Note			300	ns
t_R and t_F matching	t_{RFM}	t_R/t_F	80		120	%
Differential output signal cross-over point	V_{CRS}		1.3		2.0	V
Data transfer rate	t_{DRATE}	When the microcontroller operates at the system clock (f_X) of 6.0 MHz	1.5	1.5	1.5	Mbps
Transmission differential signal jitter	t_{UDJ1}	Upon transferring the next bit	-95	0	95	ns
	t_{UDJ2}	Upon transferring the bit following the next bit	-150	0	150	ns
Transmission EOP width	t_{EOPT1}		1.25	1.33	1.50	μs
Reception EOP width	t_{EOPR1}	EOP width to be eliminated			300	μs
	t_{EOPR2}	EOP width to be detected	675			μs
Reception USB reset width	t_{URES1}	USB reset width to be eliminated			2.5	μs
	t_{URES2}	USB reset width to be detected	5.5			μs

Note CL is the capacitance of the USBDM and USBDP output lines.

(b) Three-wire serial I/O mode (T_A = -40 to +85 °C, V_{DD} = 4.0 to 5.5 V)

(i) $\overline{\text{SCK10}}$ ...Internal clock output (when f_X = 6.0 MHz)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK10}}$ cycle time	t_{KCY1}	When TPS100[Note 1] = 0		667	667	667	ns
		When TPS100[Note 1] = 1		1,333	1,333	1,333	ns
$\overline{\text{SCK10}}$ high/low level width	t_{KH1}, t_{KL1}	When TPS100[Note 1] = 0		283	333		ns
		When TPS100[Note 1] = 1		617	667		ns
SI10 setup time	t_{SIK1}	Relative to $\overline{\text{SCK10}}$ ↑		150			ns
SI10 hold time	t_{KSI1}	Relative to $\overline{\text{SCK10}}$ ↑	When TPS100[Note 1] = 0	333			ns
			When TPS100[Note 1] = 1	667			ns
SO10 output dalay	t_{KSO1}	Relative to $\overline{\text{SCK10}}$ ↓, CL = 100 pF[Note 2]		0		200	ns

Notes 1. Bit 4 of serial operation mode register 10 (CSIM10)

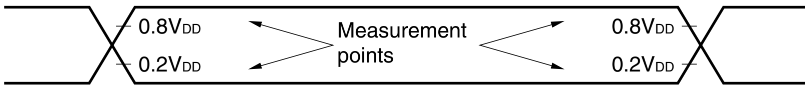
2. CL is the capacitance of the SO output line.

(ii) $\overline{\text{SCK10}}$ ...External clock output

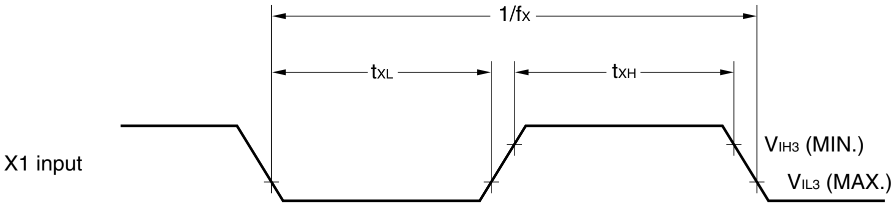
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK10}}$ cycle time	t_{KCY2}		667			ns
$\overline{\text{SCK10}}$ high/low level width	t_{KH2}, t_{KL2}		283			ns
SI10 setup time	t_{SIK2}		100			ns
SI10 hold time	t_{KSI2}		333			ns
SO10 output delay	t_{KSO2}	Relative to $\overline{\text{SCK10}}$ ↓, CL = 100 pF[Note]	0		250	ns

Note CL is the capacitance of the SO output line.

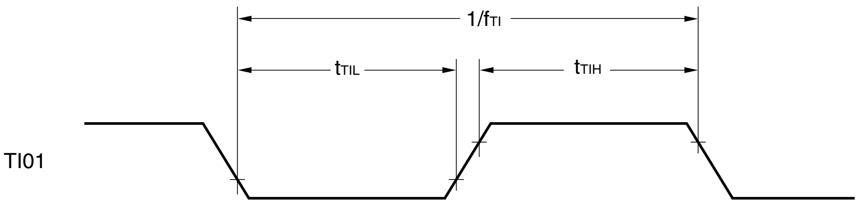
AC TIMING MEASUREMENT POINTS (except the X1 input and USB function)



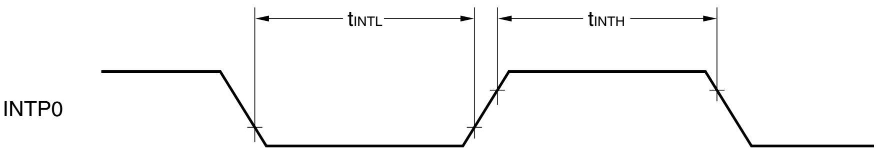
CLOCK TIMING



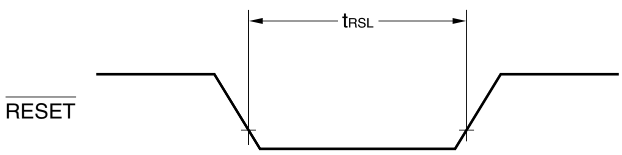
TI TIMING



INTERRUPT INPUT TIMING



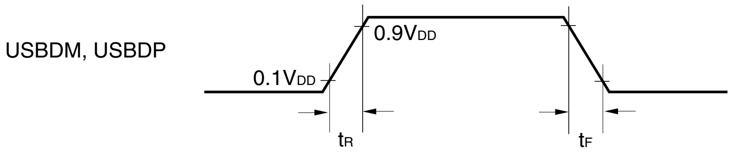
$\overline{\text{RESET}}$ INPUT TIMING



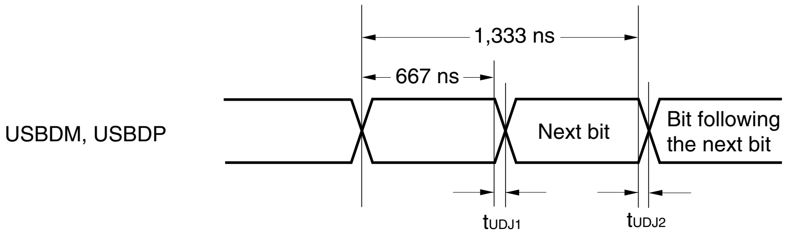
SERIAL TRANSFER TIMING

USB Function:

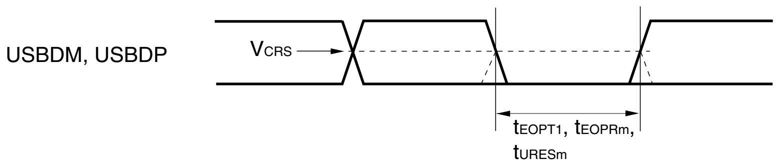
USBDM and USBDP rise/fall time



Transmission differential signal jitter

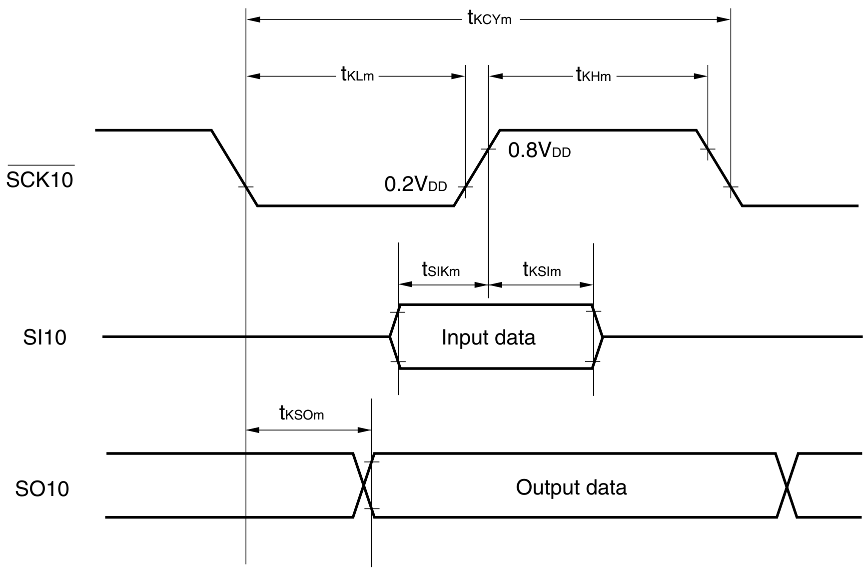


Differential output signal cross-over point, transmission EOP width, reception EOP width, and reception USB reset width



m = 1, 2

Three-Wire Serial I/O Mode:



m = 1, 2

DATA HOLD CHARACTERISTICS OF DATA MEMORY AT LOW VOLTAGE IN STOP MODE (T_A = -40 to +85 °C)

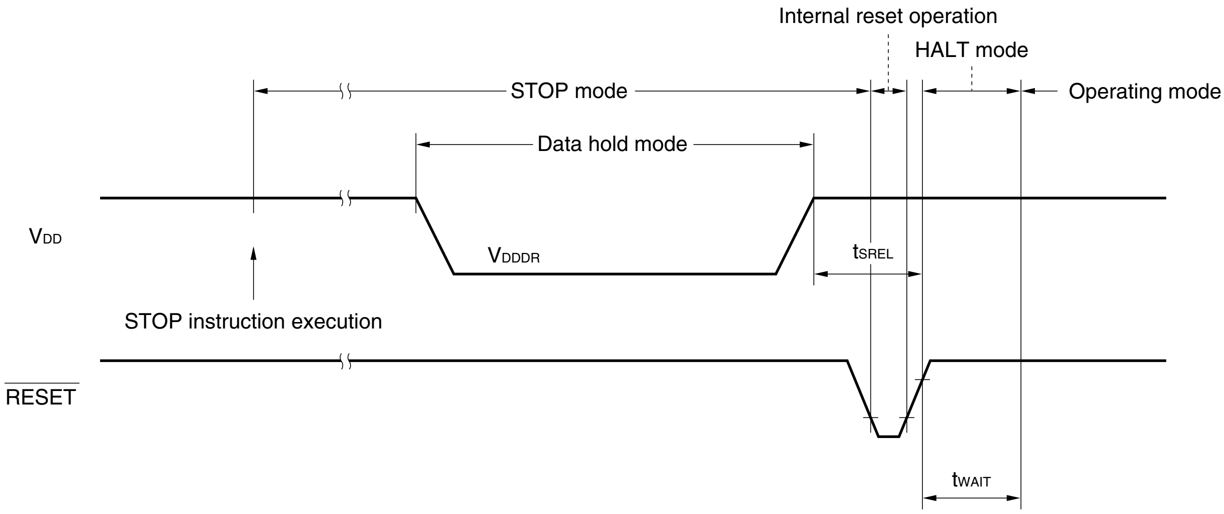
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		4.0		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation settling time Note 1	t_{WAIT}	Release by RESET		$2^{15}/f_X$		ms
		Release by interrupt request		**Note 2**		ms

Notes 1. During the oscillation settling time, CPU operations are disabled to prevent them from becoming unstable upon the start of oscillation.

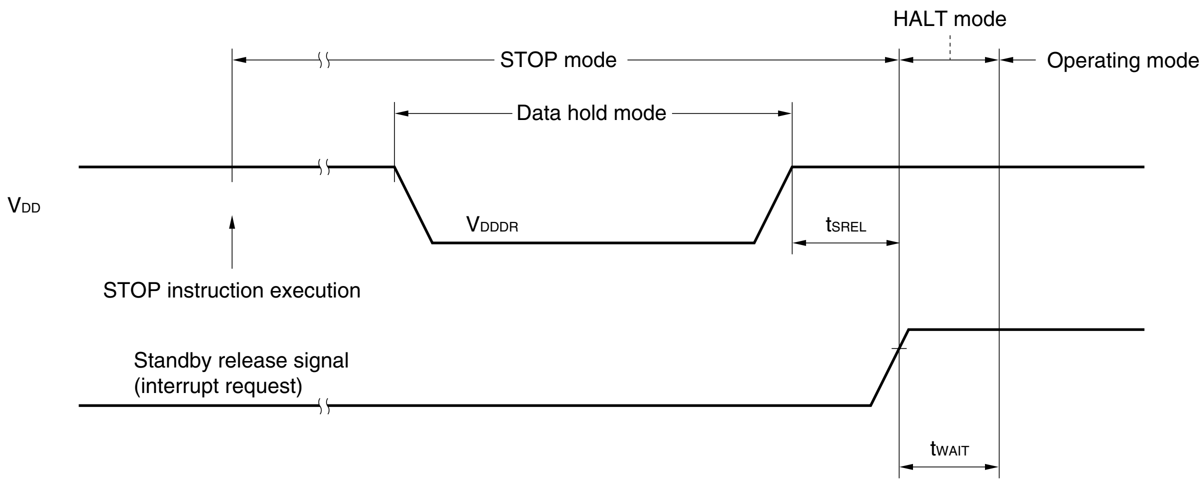
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation settling time selection register.

Remark f_X: System clock oscillation frequency

DATA HOLD TIMING (STOP mode release by RESET)

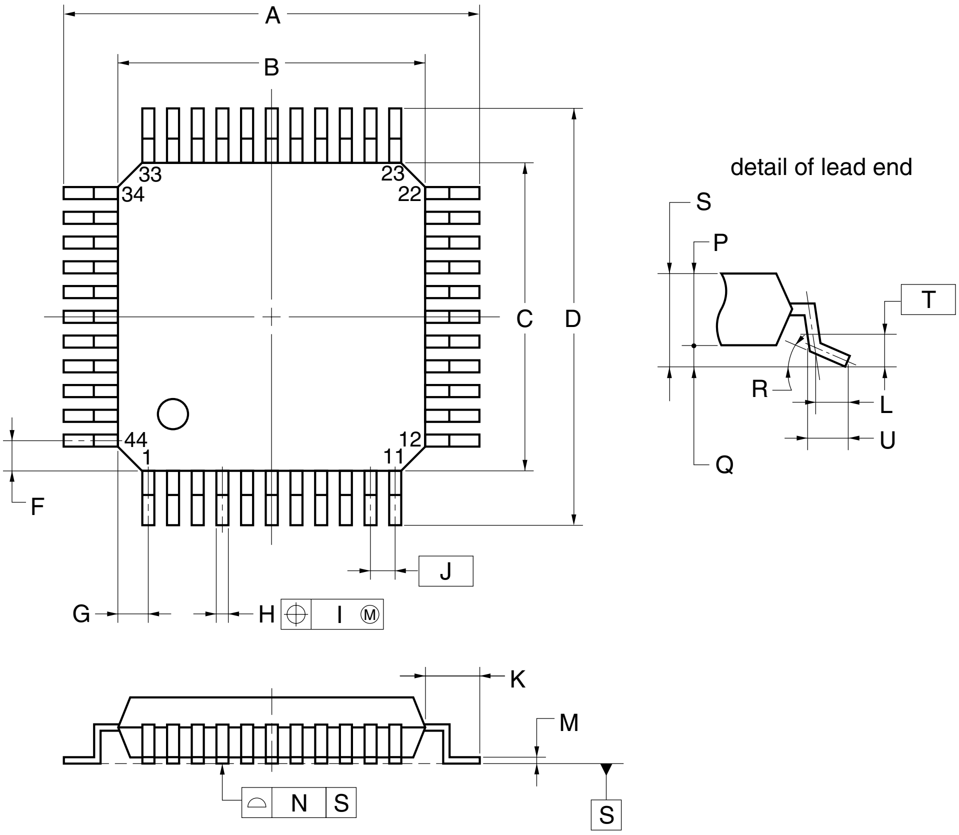


DATA HOLD TIMING (standby release signal: STOP mode release by interrupt signal)



★ 9. PACKAGE DRAWINGS

44 PIN PLASTIC QFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3°^{+4°}_{-3°}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

★ 10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9801 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual** (C10535E).

For soldering methods and conditions other than those recommended below, contact our sales representatives.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD78F9801GB-8ES: 44-pin plastic QFP (10 x 10)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235 °C Duration: 30 sec. max. (at 210 °C or above) Maximum allowable number of reflow processes: 2	IR35-00-2
VPS	Package peak temperature: 215 °C Duration: 40 sec. max. (at 200 °C or above) Maximum allowable number of reflow processes: 2	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C max. Duration: 3 sec. max. (per device side)	-

Caution Use of more than one soldering method should be avoided (except for partial heating method).

★ APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78F9801.

LANGUAGE PROCESSING SOFTWARE

RA78K0S[Notes 1, 2, 3]	Assembler package common to the 78K/0S series
CC78K0S[Notes 1, 2, 3]	C compiler package common to the 78K/0S series
DF789801[Notes 1, 2, 3]	Device file for the μPD789800 sub-series
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to the 78K/0S series

FLASH MEMORY WRITE TOOLS

Flashpro III (Model number: FL-PR3[Note 4], PG-FP3)	Dedicated flash writer
FA-44GB-8ES[Note 4]	Flash memory write adapter (GB-8ES type)

DEBUGGING TOOLS (1/2)

IE-78K0S-NS In-circuit Emulator	In-circuit emulator for debugging hardware and software of application system using 78K/0S Series. Supports integrated debugger (ID78K0S-NS). Used in combination with AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-78K0S-NS-A In-circuit Emulator	A coverage function is added to the IE-78K0S-NS, and the tracer and timer functions are improved to enhance debugging.
IE-70000-MC-PS-B AC Adapter	This is the adapter for supplying power from outlet of 100 to 240 VAC.
IE-70000-98-IF-C Interface Adapter	This adapter is needed when PC-9800 series (excluding notebook models) is used as a host machine of IE-78K0S-NS. (Compatible with C bus)
IE-70000-CD-IF-A PC Card Interface	This PC card and interface cable are needed when a notebook-type personal computer is used as a host machine of IE-78K0S-NS. (Compatible with a PCMCIA socket)
IE-70000-PC-IF-C Interface Adapter	This adapter is needed when IBM PC/AT™ and compatibles are used as a host machine of IE-78K0S-NS. (Compatible with ISA bus)
IE-70000-PCI-IF-A Interface Adapter	This adapter is needed when a personal computer with a built-in PCI bus is used as a host machine of IE-78K0S-NS.
IE-789801-NS-EM1 Emulation Board	Emulation board for emulating the peripheral hardware inherent to the device. Used in combination with in-circuit emulator.

Notes 1. Based on the PC-9800 series (Japanese Windows™)
2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)
3. Based on the HP9000 series 700™ (HP-UX™), and SPARCstation™ (SunOS™, Solaris™)
4. Product manufactured by Naito Densei Machida Mfg. Co., Ltd. (045-475-4191).

Remark The RA78K0S and CC78K0S can be used in combination with the DF789801.

DEBUGGING TOOLS (2/2)

NP-44GB-TQ[Note 1] Emulation Probe		This probe is used to connect the in-circuit emulator to the target system and is designed for 44-pin plastic QFP. Used in combination with TGB-044SAP.
	TGB-044SAP[Note 2] Conversion Socket	This conversion socket connects the NP-44GB-TQ to the target system board designed to mount a 44-pin plastic QFP (GB-8ES type).
SM78K0S[Notes 3, 4]		System simulator common to the 78K/0S series
ID78K0S-NS[Notes 3, 4]		Integrated debugger common to the 78K/0S series
DF789801[Notes 3, 4]		Device file for the μPD789800 sub-series

Notes 1. Product manufactured by Naito Densei Machida Mfg. Co., Ltd. (045-475-4191). Contact an NEC sales representative for purchase.

2. Product manufactured by TOKYO ELETEC Corporation
For further information, consult:
Tokyo Electronic Div. (TEL (03) 3820-7112), or
Osaka Electronic Div. (TEL (06) 6244-6672)
Daimaru Kogyo Corporation.

3. Based on the PC-9800 series (Japanese Windows)

4. Based on the IBM PC/AT and compatibles (Japanese/English Windows)

Remark The SM78K0S can be used in combination with the DF789801.

★ APPENDIX B RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789800 Data Sheet	U12627E
μPD78F9801 Data Sheet	This document
μPD789800 Subseries User's Manual	U12978E
78K/0S Series User's Manual, Instruction	U11047E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U14876E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U14871E
	Language	U14872E
SM78K0S, SM78K0 System Simulator Ver.2.10 or Later	Operation (Windows Based)	U14611E
SM78K Series System Simulator Ver.2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver.2.20 or Later	Operation (Windows Based)	U14910E
Project Manager Ver.3.12 or Later (Windows Based)		U14610E

Documents Related To Development Tools (Hardware) (User's Manual)

Document Name	Document No.
IE-78K0S-NS In-circuit Emulator	U13549E
IE-78K0S-NS-A In-circuit Emulator	U15207E
IE-789801-NS-EM1 Emulation Board	U13390E

Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

[MEMO]

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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