NEC

MOS INTEGRATED CIRCUIT

μPD17P709A

4-BIT SINGLE-CHIP MICROCONTROLLER WITH DEDICATED HARDWARE FOR DIGITAL TUNING SYSTEM

DESCRIPTION

The μPD17P709A is produced by replacing the on-chip mask ROM of the μPD17704A, 17705A, 17707A, 17708A, and 17709A with a one-time PROM.

The μPD17P709A allows programs to be written once, so the μPD17P709A is suitable for preproduction in μPD17704A, 17705A, 17707A, 17708A, or 17709A system development or low-volume production.

When reading this document, also refer to the publications on the μPD17704A, 17705A, 17707A, 17708A, or 17709A.

The electrical characteristics (including power supply current) and PLL analog characteristics of the μPD17P709A differ from those of the μPD17704A, 17705A, 17707A, 17708A, and 17709A. In high-volume application set production, be sure to carefully check these differences.

FEATURES

- Compatible with the μPD17704A, 17705A, 17707A, 17708A, and 17709A
- On-chip one-time PROM: 32 KB (16384 × 16 bits)
- Supply voltage: V_{DD} = 5 V ±10%

ORDERING INFORMATION

Part Number	Package
μPD17P709AGC-3B9	80-pin plastic QFP (14 × 14)

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Printed in Japan

FUNCTIONAL OUTLINE

(1/2)

Item \ Part Number	μPD17704A	μPD17705A	μPD17707A	μPD17708A	μPD17709A	μPD17P709A
Program memory (ROM)	8192 × 16 bits (mask ROM)	12288 × 16 bits (mask ROM)		16384 × 16 bits (mask ROM)		16384 × 16 bits (one-time PROM)
General-purpose data memory (RAM)	672 × 4 bits		1120 × 4 bits		1176 × 4 bits	
Instruction execution time	1.78 μs (with f_X = 4.5 MHz crystal oscillator)					
General-purpose ports	• I/O ports: 46 • Input ports: 12 • Output ports: 4					
Stack levels	• Address stack: 15 levels • Interrupt stack: 4 levels • DBF stack: 4 levels (can be manipulated via software)					
Interrupts	• External: 6 sources (falling edge of CE pin, INT0 to INT4) • Internal: 6 sources (timers 0 to 3, serial interfaces 0 and 1)					
Timer	5 channels • Basic timer (clock: 10, 20, 50, 100 Hz): 1 channel • 8-bit timer with gate counter (clock: 1 k, 2 k, 10 k, 100 kHz): 1 channel • 8-bit timer (clock: 1 kHz, 2 kHz, 10 kHz, 100 kHz): 2 channels • 8-bit timer multiplexed with PWM (clock: 440 Hz, 4.4 kHz): 1 channel					
A/D converter	8 bits × 6 channels (hardware mode and software mode selectable)					
D/A converter (PWM)	3 channels (8-bit or 9-bit resolution selectable by software) Output frequency: 4.4 kHz, 440 Hz (with 8-bit PWM selected) 2.2 kHz, 220 Hz (with 9-bit PWM selected)					
Serial interface	2 units (3 channels) • 3-wire serial I/O: 2 channels • 2-wire serial I/O/I^2C bus: 1 channel					
PLL — Division mode	• Direct division mode (VCOL pin (MF mode): 0.5 to 3 MHz) • Pulse swallow mode (VCOL pin (HF mode): 10 to 40 MHz) (VCOH pin (VHF mode): 60 to 130 MHz)					
PLL — Reference frequency	13 types selectable (1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 18, 20, 25, 50 kHz)					
PLL — Charge pump	Two error-out output pins (EO0, EO1)					
PLL — Phase comparator	Unlock status detectable by program					
Intermediate frequency counter	• Intermediate frequency (IF) measurement P1C0/FMIFC pin: 10 to 11 MHz in FMIF mode 0.4 to 0.5 MHz in AMIF mode P1C1/AMIFC pin: 0.4 to 0.5 MHz in AMIF mode • External gate width measurement P2A1/FCG1, P2A0/FCG0 pin					
BEEP output	2 pins Output frequency: 1 kHz, 3 kHz, 4 kHz, 6.7 kHz (BEEP0 pin) 67 Hz, 200 Hz, 3 kHz, 4 kHz (BEEP1 pin)					

(2/2)

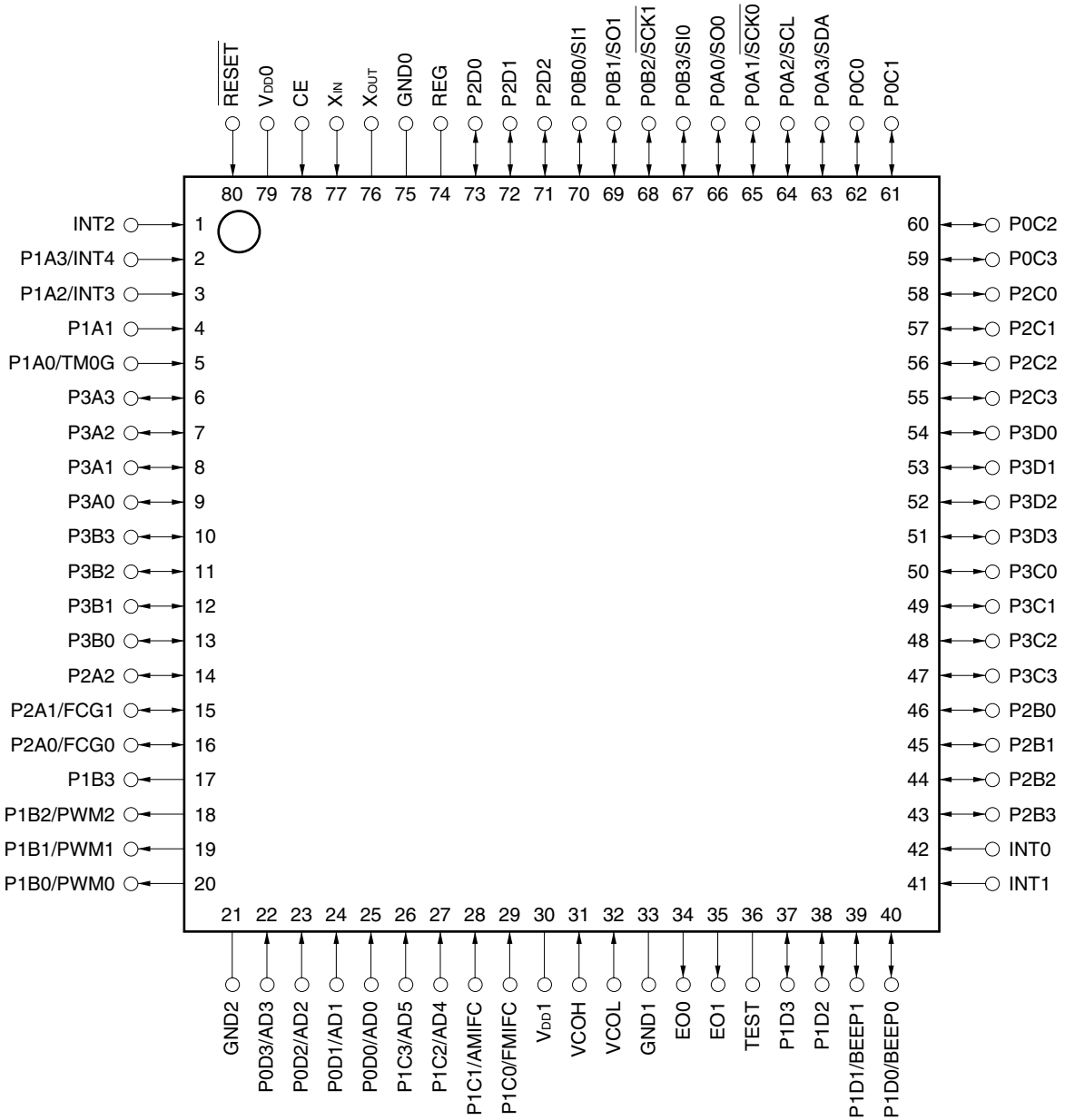
Item \ Part Number	μPD17704A	μPD17705A	μPD17707A	μPD17708A	μPD17709A	μPD17P709A
Reset	• Power-on reset (on power application) • Reset by $\overline{\text{RESET}}$ pin • Watchdog timer reset Can be set only once on power application: 65536 instructions, 131072 instructions, or no-use selectable • Stack pointer overflow/underflow reset Can be set only once on power application: interrupt stack or address stack selectable • CE reset (CE pin low → high level) CE reset delay timing can be set. • Power failure detection function					
Standby	• Clock stop mode (STOP) • Halt mode (HALT)					
Supply voltage	• PLL operation: V_{DD} = 4.5 to 5.5 V • CPU operation: V_{DD} = 3.5 to 5.5 V					
Package	80-pin plastic QFP (14 × 14)					

PIN CONFIGURATION (TOP VIEW)

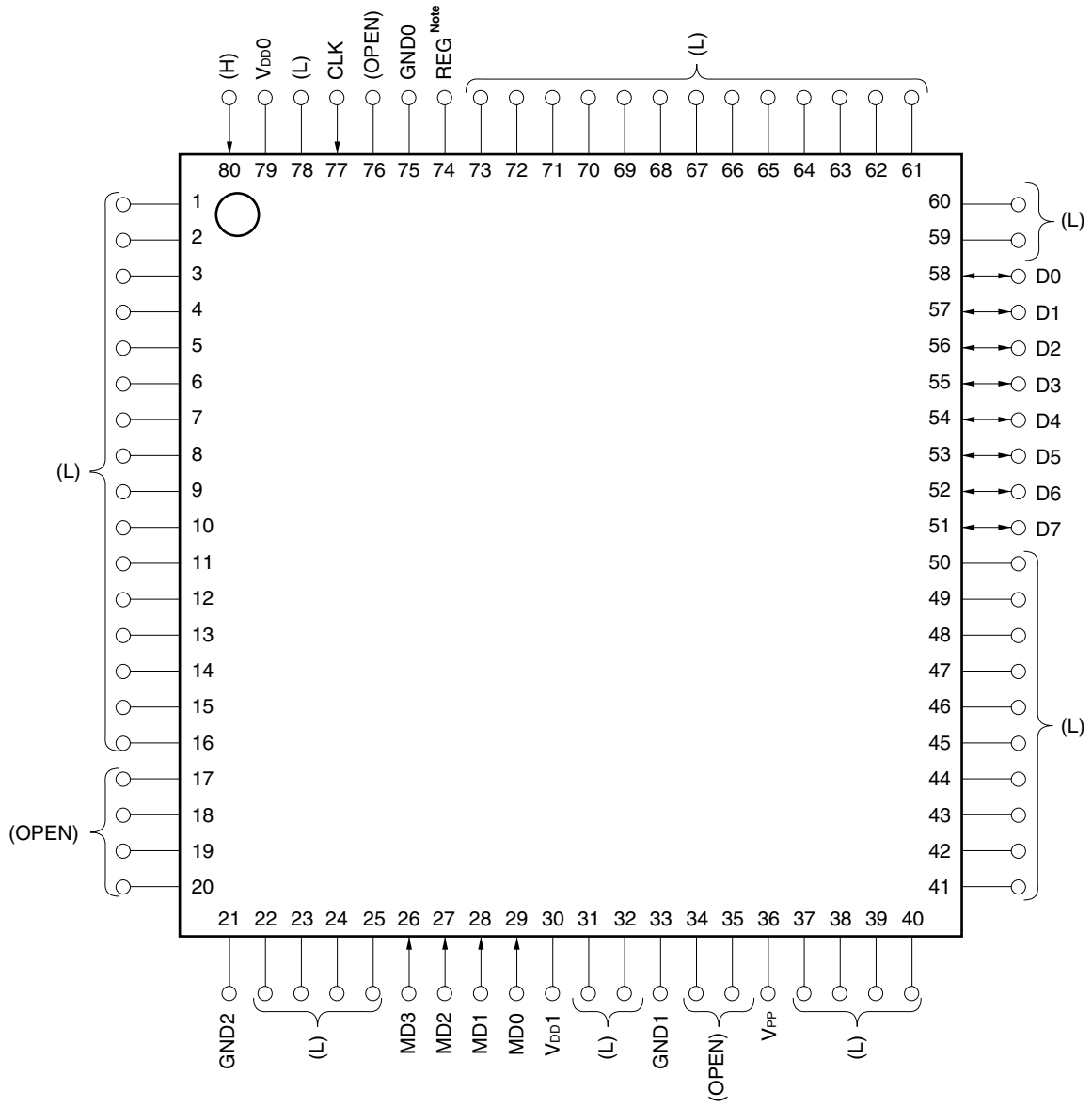
80-pin plastic QFP (14 × 14)

μPD17P709AGC-3B9

(1) Normal operation mode



(2) PROM programming mode



Note Connect to the same potential as V_{DD}.

Caution The items in parentheses indicate the processing of pins not used in the PROM programming mode.

L: Independently connect to GND via a resistor (470 Ω)

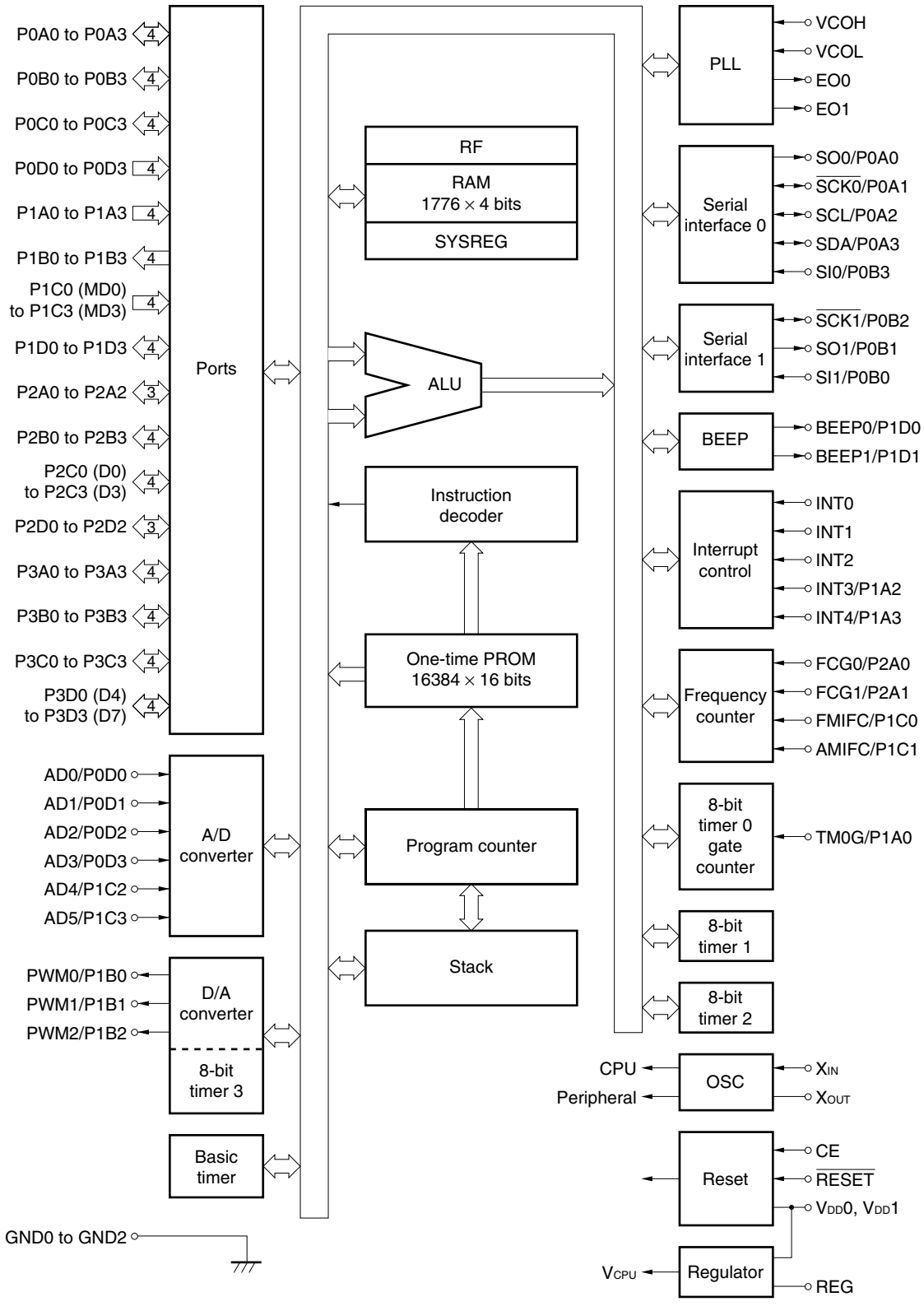
H: Independently connect each pin to V_{DD} via a resistor (470 Ω)

OPEN: Leave open.

PIN NAMES

AD0 to AD5:	A/D converter input	P2B0 to P2B3:	Port 2B
AMIFC:	AM frequency counter input	P2C0 to P2C3:	Port 2C
BEEP0, BEEP1:	BEEP output	P2D0 to P2D2:	Port 2D
CE:	Chip enable	P3A0 to P3A3:	Port 3A
CLK:	Address update clock input	P3B0 to P3B3:	Port 3B
D0 to D7:	Data I/O	P3C0 to P3C3:	Port 3C
EO0, EO1:	Error-out output	P3D0 to P3D3:	Port 3D
FCG0, FGC1:	Frequency counter gate input	REG:	CPU regulator
FMIFC:	FM frequency counter input	$\overline{\text{RESET}}$:	Reset input
GND0 to GND2:	Ground 0 to 2	$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$:	3-wire serial clock I/O
INT0 to INT4:	External interrupt input	SCL:	2-wire serial clock I/O
MD0 to MD3:	Operation mode selection	SDA:	2-wire serial data I/O
PWM0 to PWM2:	D/A converter output	SI0, SI1:	3-wire serial data input
P0A0 to P0A3:	Port 0A	SO0, SO1:	3-wire serial data output
P0B0 to P0B3:	Port 0B	TEST:	Test input
P0C0 to P0C3:	Port 0C	TM0G:	Timer 0 gate input
P0D0 to P0D3:	Port 0D	VCOH:	Local oscillation high input
P1A0 to P1A3:	Port 1A	VCOL:	Local oscillation low input
P1B0 to P1B3:	Port 1B	$V_{DD}0$, $V_{DD}1$:	Power supply
P1C0 to P1C3:	Port 1C	V_{PP}:	Program voltage application
P1D0 to P1D3:	Port 1D	X_{IN}, X_{OUT}:	Main clock oscillation
P2A0 to P2A2:	Port 2A		

BLOCK DIAGRAM



Remark Pins in parentheses are used in PROM programming mode.

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Function List

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th><th>Output Form</th></tr>
<tr><td>1
41
42</td><td>INT2
INT1
INT0</td><td>Edge-detectable vectored interrupt input pins. Rising or falling edge can be specified.</td><td>–</td></tr>
<tr><td>2
3
4
5</td><td>P1A3/INT4
P1A2/INT3
P1A1
P1A0/TM0G</td><td>Port 1A multiplexed with external interrupt request signal input and event signal input pins.
• P1A3 to P1A0
  • 4-bit input port
• INT4, INT3
  • Edge-detectable vectored interrupt
• TM0G
  • Input for gate of 8-bit timer 0
<table><tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>Input
(P1A3 to P1A0)</td><td>Input
(P1A3 to P1A0)</td><td>Retained</td><td>Retained</td></tr></table></td><td>–</td></tr>
<tr><td>6
|
9</td><td>P3A3
|
P3A0</td><td>4-bit I/O port.
Input or output can be specified in 4-bit units.
<table><tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr></table></td><td>CMOS
push-pull</td></tr>
<tr><td>10
|
13</td><td>P3B3
|
P3B0</td><td>4-bit I/O port.
Input or output can be specified in 4-bit units.
<table><tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr></table></td><td>CMOS
push-pull</td></tr>
<tr><td>14
15
16</td><td>P2A2
P2A1/FCG1
P2A0/FCG0</td><td>Port 2A multiplexed with external gate counter input pins.
• P2A2 to P2A0
  • 3-bit I/O port
  • Input or output can be specified in 1-bit units.
• FCG1, FCG0
  • Input for external gate counter
<table><tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr><tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr><tr><td>Input
(P2A2 to P2A0)</td><td>Input
(P2A2 to P2A0)</td><td>Retained
(P2A2 to P2A0)</td><td>Retained
(P2A2 to P2A0)</td></tr></table></td><td>CMOS
push-pull</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Symbol</th><th colspan="4">Function</th><th>Output Form</th></tr>
<tr><td rowspan="4">17
18
|
20</td><td rowspan="4">P1B3
P1B2/PWM2
|
P1B0/PWM0</td><td colspan="4">Port 1B multiplexed with D/A converter output pins.
• P1B3 to P1B0
• 4-bit output port
• PWM2 to P2M0
• 8- or 9-bit D/A converter output</td><td rowspan="4">N-ch open-drain (12 V withstanding voltage)</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Outputs low level (P1B3 to P1B0)</td><td>Outputs low level (P1B3 to P1B0)</td><td>Retained</td><td>Retained (P1B3 to P1B0)</td></tr>
<tr><td>21
33
75</td><td>GND2
GND1
GND0</td><td colspan="4">Ground</td><td>–</td></tr>
<tr><td rowspan="4">22
|
25</td><td rowspan="4">P0D3/AD3
|
P0D0/AD0</td><td colspan="4">Port 0D multiplexed with A/D converter input pins
• P0D3 to P0D0
• 4-bit input port
• Pull-down resistors can be connected in 1-bit units.
• AD3 to AD0
• Analog input of A/D converter with 8-bit resolution</td><td rowspan="4">–</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input with pull-down resistor (P0D3 to P0D0)</td><td>Input with pull-down resistor (P0D3 to P0D0)</td><td>Retained</td><td>Retained</td></tr>
<tr><td rowspan="4">26
27
28
29</td><td rowspan="4">P1C3/AD5
P1C2/AD4
P1C1/AMIFC
P1C0/FMIFC</td><td colspan="4">Port 1C multiplexed with A/D converter input and IF counter input pins.
• P1C3 to P1C0
• 4-bit input port
• AD5, AD4
• Analog input to A/D converter with 8-bit resolution
• FMIFC, AMIFC
• Input to frequency counter</td><td rowspan="4">–</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input (P1C3 to P1C0)</td><td>Input (P1C3 to P1C0)</td><td>• P1C3/AD5, P1C2/AD4 Retained
• P1C1/AMIFC, P1C0/FMIFC Input (P1C1, P1C0)</td><td>• P1C3/AD5, P1C2/AD4 Retained
• P1C1/AMIFC, P1C0/FMIFC Input (P1C1, P1C0)</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Function</th><th>Output Form</th></tr>
<tr><td>30
79</td><td>$V_{DD}1$
$V_{DD}0$</td><td>Power supply. Supply the same voltage to these pins.
• With CPU and peripheral function operating: 4.5 to 5.5 V
• With CPU operating: 3.5 to 5.5 V
• With clock stopped: 2.2 to 5.5 V</td><td>–</td></tr>
<tr><td>31
32</td><td>VCOH
VCOL</td><td>PLL local oscillation (VCO) frequency input.
• VCOH
• Active with VHF mode selected by program; otherwise, pulled down.
• VCOL
• Active with HF or MW mode selected by program; otherwise, pulled down.

Because the input of these pins goes into an AC amplifier, cut the DC component of the input signal with a capacitor.</td><td>–</td></tr>
<tr><td rowspan="4">34
35</td><td rowspan="4">EO0
EO1</td><td colspan="4">Output from charge pump of PLL frequency synthesizer. Outputs the divided frequency of local oscillation and the result of comparison of the phase difference of the reference frequency.</td><td rowspan="4">CMOS
3-state</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>High-impedance output</td><td>High-impedance output</td><td>High-impendance output</td><td>High-impedance output</td></tr>
<tr><td>36</td><td>TEST</td><td colspan="4">Test input pin.
Be sure to connect this pin to GND.</td><td>–</td></tr>
<tr><td rowspan="4">37
38
39
40</td><td rowspan="4">P1D3
P1D2
P1D1/BEEP1
P1D0/BEEP0</td><td colspan="4">Port 1D and BEEP output.
• P1D3 to P1D0
• 4-bit I/O port
• Input or output can be specified in 1-bit units.
• BEEP1, BEEP0
• BEEP output</td><td rowspan="4">CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input
(P1D3 to P1D0)</td><td>Input
(P1D3 to P1D0)</td><td>Retained
(P1D3 to P1D0)</td><td>Retained
(P1D3 to P1D0)</td></tr>
<tr><td rowspan="4">43
|
46</td><td rowspan="4">P2B3
|
P2B0</td><td colspan="4">4-bit I/O port.
Input or output can be specified in 1-bit units.</td><td rowspan="4">CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr>
<tr><td rowspan="4">47
|
50</td><td rowspan="4">P3C3
|
P3C0</td><td colspan="4">4-bit I/O port.
Input or output can be specified in 4-bit units.</td><td rowspan="4">CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Symbol</th><th colspan="4">Function</th><th>Output Form</th></tr>
<tr><td rowspan="4">51
|
54</td><td rowspan="4">P3D3
|
P3D0</td><td colspan="4">4-bit I/O port.
Input or output can be specified in 4-bit units.</td><td rowspan="4">CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr>
<tr><td rowspan="4">55
|
58</td><td rowspan="4">P2C3
|
P2C0</td><td colspan="4">4-bit I/O port.
Input or output can be specified in 4-bit units.</td><td rowspan="4">CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr>
<tr><td rowspan="4">59
|
62</td><td rowspan="4">P0C3
|
P0C0</td><td colspan="4">4-bit I/O port.
Input or output can be specified in 4-bit units.</td><td rowspan="4">CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr>
<tr><td>63
64</td><td>P0A3/DSA
P0A2/SCL</td><td colspan="4" rowspan="5">Ports P0A and P0B are multiplexed with I/O of serial interface.
• P0A3 to P0A0
• 4-bit I/O port
• Input or output can be specified in 1-bit units.
• P0B3 to P0B0
• 4-bit I/O port
• Input or output can be specified in 1-bit units.
• SDA, SCL
• Serial data and serial clock I/O of serial interface 0 in 2-wire serial I/O or I²C bus mode
• $\overline{SCK0}$, SO0, SI0
• Serial clock I/O, serial data output, and serial data input of serial interface 0 in 3-wire serial I/O mode
• $\overline{SCK1}$, SO1, SI1
• Serial clock I/O, serial data output, serial data input of serial interface 1 in 3-wire serial I/O mode</td><td>N-ch
open-drain</td></tr>
<tr><td rowspan="4">65
66
67
68
69
70</td><td rowspan="4">P0A1/$\overline{SCK0}$
P0A0/SO0
P0B3/SI0
P0B2/$\overline{SCK1}$
P0B1/SO1
P0B0/SI1</td><td>CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input
(P0A3 to P0A0,
P0B3 to P0B0)</td><td>Input
(P0A3 to P0A0,
P0B3 to P0B0)</td><td>Retained
(P0A3 to P0A0,
P0B3 to P0B0)</td><td>Retained
(P0A3 to P0A0,
P0B3 to P0B0)</td></tr>
<tr><td rowspan="4">71
|
73</td><td rowspan="4">P2D2
|
P2D0</td><td colspan="4">3-bit I/O port.
Input or output can be specified in 1-bit units.</td><td rowspan="4">CMOS
push-pull</td></tr>
<tr><td colspan="3">After reset</td><td rowspan="2">With clock stopped</td></tr>
<tr><td>Power-on reset</td><td>WDT&SP reset</td><td>CE reset</td></tr>
<tr><td>Input</td><td>Input</td><td>Retained</td><td>Retained</td></tr>
</table>

Pin No.	Symbol	Function	Output Form
74	REG	CPU regulator. Connect this pin to GND via 0.1 μF capacitor.	–
76 77	X_{OUT} X_{IN}	Ground pins of crystal resonator.	–
78	CE	Device operation selection, CE reset, and interrupt signal input pin. • Device operation selection When CE is high, the PLL frequency synthesizer can operate. When CE is low, the PLL frequency synthesizer is automatically disabled internally. • CE reset When CE goes high, the device is reset at the rising edge of the internal basic timer setting pulse. This pin also has a reset timing delay function. • Interrupt A vectored interrupt occurs at the falling edge of this pin.	–
80	$\overline{\text{RESET}}$	Reset input	–

1.2 PROM Programming Mode

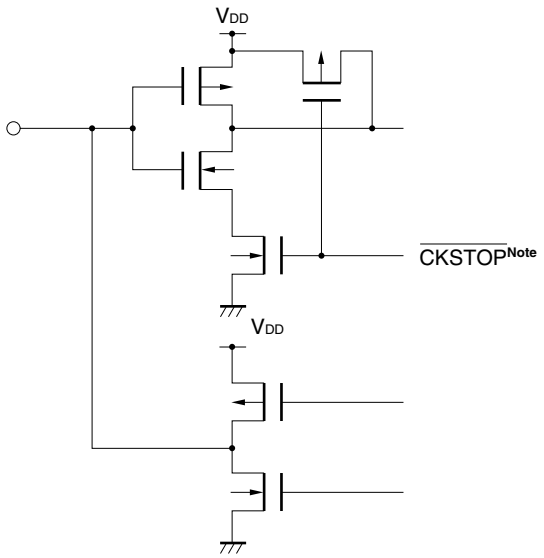
Pin No.	Symbol	Function	Output Form
26 | 29	MD3 | MD0	Input for operating mode selection for program memory write, read, or verify.	–
21 33 75	GND2 GND1 GND0	Ground	–
36	V_{PP}	Pin to which program voltage is applied during program memory write, read, or verify. +12.5 V is applied.	–
30 79	$V_{DD}1$ $V_{DD}0$	Power supply pins. +6 V is applied during program memory write, read, or verify.	–
51 | 58	D7 | D0	8-bit data I/O for program memory write, read, or verify	CMOS push-pull
77	CLK	Clock input for address updating during program memory write, read, or verify	–

Remark The pins other than those listed above are not used in PROM programming mode. For the handling of the unused pins, see **PIN CONFIGURATION (2) PROM programming mode**.

1.3 Equivalent Circuits of Pins

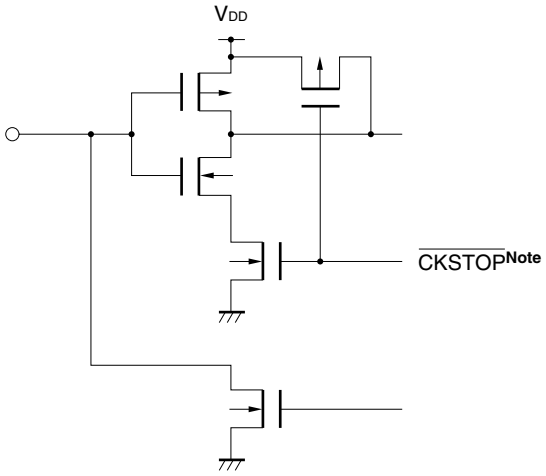
(1) P0A (P0A1/$\overline{SCK0}$, P0A0/SO0)
P0B (P0B3/SI0, P0B2/$\overline{SCK1}$, P0B1/SO1, P0B0/SI1)
P0C (P0C3, P0C2, P0C1, P0C0)
P1D (P1D3, P1D2, P1D1/BEEP1, P1D0/BEEP0)
P2A (P2A2, P2A1/FCG1, P2A0/FCG0)
P2B (P2B3, P2B2, P2B1, P2B0)
P2C (P2C3, P2C2, P2C1, P2C0)
P2D (P2D2, P2D1, P2D0)
P3A (P3A3, P3A2, P3A1, P3A0)
P3B (P3B3, P3B2, P3B1, P3B0)
P3C (P3C3, P3C2, P3C1, P3C0)
P3D (P3D3, P3D2, P3D1, P3D0)

(I/O)



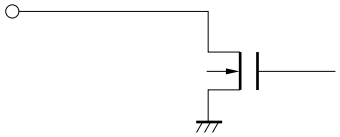
Note This is an internal signal that is output when the clock stop instruction is executed. Its circuit is designed not to increase the current consumption due to noise even if it is floated.

(2) P0A (P0A3/SDA, P0A2/SCL) (I/O)

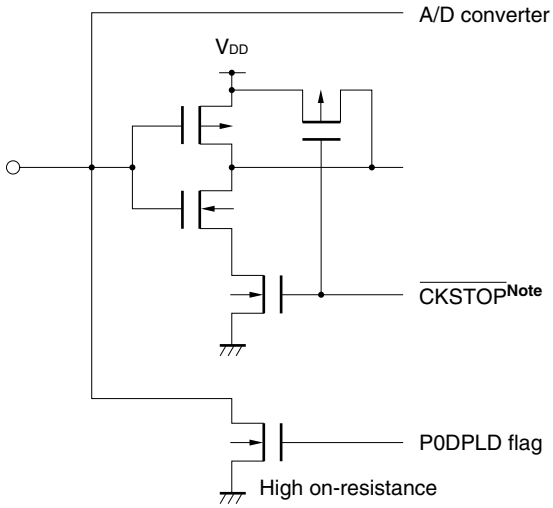


Note This is an internal signal that is output when the clock stop instruction is executed. Its circuit is designed not to increase the current consumption due to noise even if it is floated.

(3) P1B (P1B3, P1B2/PWM2, P1B1/PWM1, P1B0/PWM0) (output)

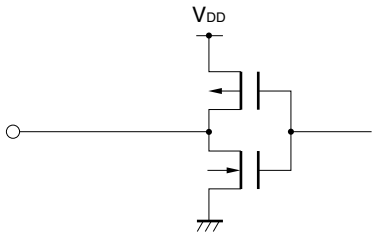


(4) P0D (P0D3/AD3, P0D2/AD2, P0D1/AD1, P0D0/AD0) (input)

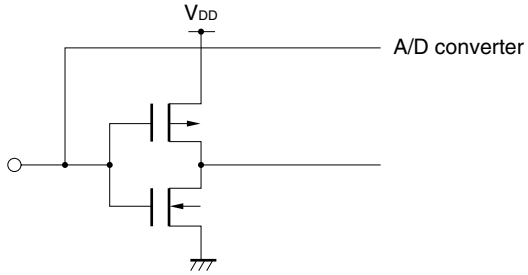


Note This is an internal signal that is output when the clock stop instruction is executed. Its circuit is designed not to increase the current consumption due to noise even if it is floated.

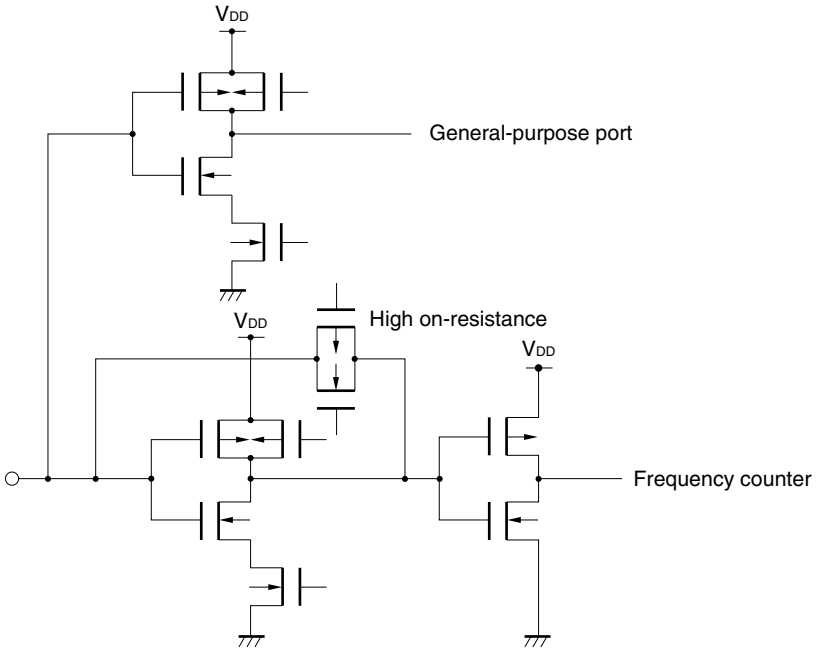
(5) P1A (P1A1) (input)



(6) P1C (P1C3/AD5, P1C2/AD4) (input)

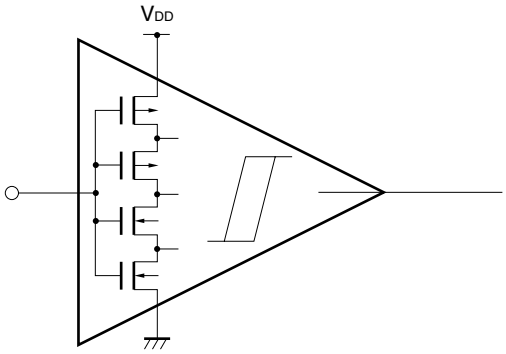


(7) P1C (P1C1/AMIFC, P1C0/FMIFC) (input)

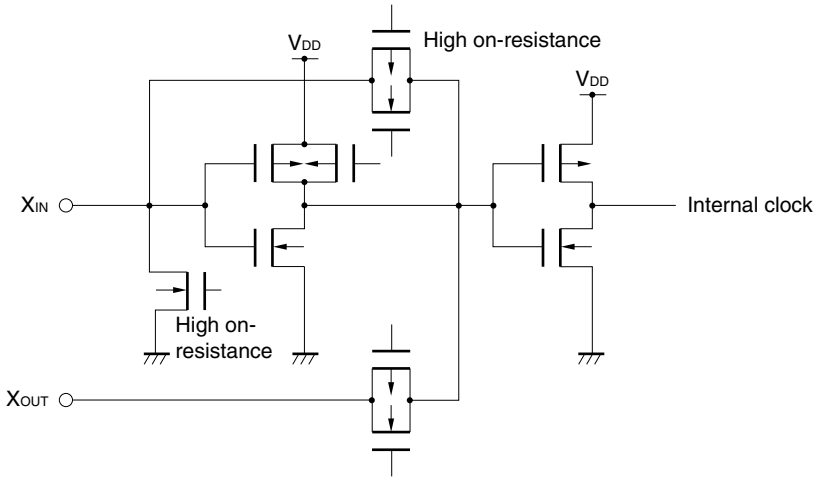


(8) CE

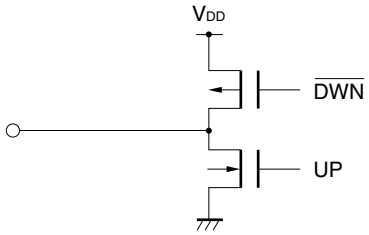
$\overline{\text{RESET}}$
INT0, INT1, INT2
P1A (P1A3/INT4, P1A2/INT3, P1A0/TM0G)
} **(Schmitt-triggered input)**



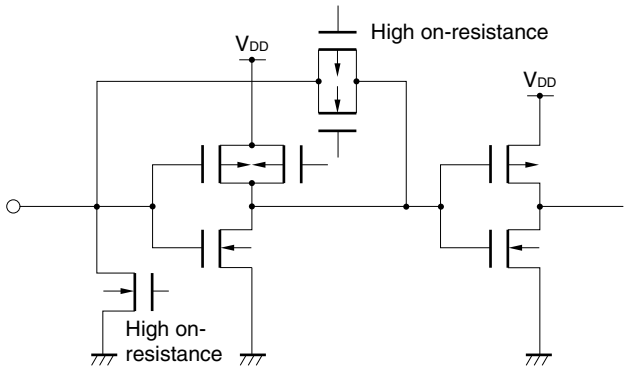
(9) XOUT (output), XIN (input)



(10) EO1, EO0 (output)



(11) VCOH, VCOL (input)



1.4 Connections of Unused Pins

It is recommended to connect unused pins as follows.

Table 1-1. Connections of Unused Pins

(1/2)

Pin Name		I/O Mode	Recommended Connection
Port pin	P0D3/AD3 to P0D0/AD0	Input	Independently connect to GND via a resistor[Note 1].
	P1C3/AD5 P1C2/AD4		
	P1C1/AMIFC[Note 2] P1C0/FMIFC[Note 2]		Set to port mode and individually connect to V_{DD} or GND via a resistor[Note 1].
	P1A3/INT4 P1A2/INT3 P1A1 P1A0/TM0G		Independently connect to GND via a resistor[Note 1].
	P1B3 P1B2/PWM2 to P1B0/PWM0	N-ch open-drain output	Set to low-level output by software and leave open.
	P0A3/SDA P0A2/SCL P0A1/$\overline{SCK0}$ P0A0/SO0	I/O[Note 3]	Set to general-purpose input port mode by software and independently connect to V_{DD} or GND via a resistor[Note 1].
	P0B3/SI0 P0B2/$\overline{SCK1}$ P0B1/SO1 P0B0/SI1		
	P0C3 to P0C0		
	P1D3 P1D2 P1D1/BEEP1 P1D0/BEEP0		
	P2A2 P2A1/FCG1 P2A0/FCG0		
	P2B3 to P2B0		
	P2C3 to P2C0		
	P2D2 to P2D0		

Notes 1. If a pin is externally pulled up (connected to V_{DD} via a resistor) or pulled down (connected to GND via a resistor) with a high resistance, the pin almost enters a high-impedance state, increasing the current (through-current) consumption of the port. Generally, the resistance of a pull-up or pull-down resistor is several 10 kΩ, although it depends on the application circuit.

2. Do not set these pins as AMIFC and FMIFC pins; otherwise, the current consumption will increase.

3. The I/O ports are set in the general-purpose input port mode at power-on reset, when reset by the $\overline{RESET}$ pin, or when reset by an overflow or underflow of the watchdog timer or the stack.

Table 1-1. Connections of Unused Pins

(2/2)

Pin Name		I/O Mode	Recommended Connection
Port pin	P3A3 to P3A0	I/O[Note 2]	Set in general-purpose input port mode by software and independently connect to V_{DD} or GND via a resistor[Note 1].
	P3B3 to P3B0		
	P3C3 to P3C0		
	P3D3 to P3D0		
Non-port pins	CE	Input	Connect to V_{DD} via a resistor[Note 1].
	EO1	Output	Leave open.
	EO0		
	INT0 to INT2	Input	Independently connect to GND via a resistor[Note 1].
	$\overline{\text{RESET}}$	Input	Connect to V_{DD} via a resistor[Note 1].
	TEST	–	Directly connect to GND.
	VCOH	Input	Disable PLL via software and leave open.
	VCOL		

Notes 1. If a pin is externally pulled up (connected to V_{DD} via a resistor) or pulled down (connected to GND via a resistor) with a high resistance, the pin almost enters a high-impedance state, increasing the current (through-current) consumption of the port. Generally, the resistance of a pull-up or pull-down resistor is several 10 kΩ, although it depends on the application circuit.

2. The I/O ports are set in the general-purpose input port mode at power-on reset, when reset by the $\overline{\text{RESET}}$ pin, or when reset by an overflow or underflow of the watchdog timer or the stack.

1.5 Cautions on Using CE, INT0 to INT4, and $\overline{\text{RESET}}$ Pins (Only in Normal Operation Mode)

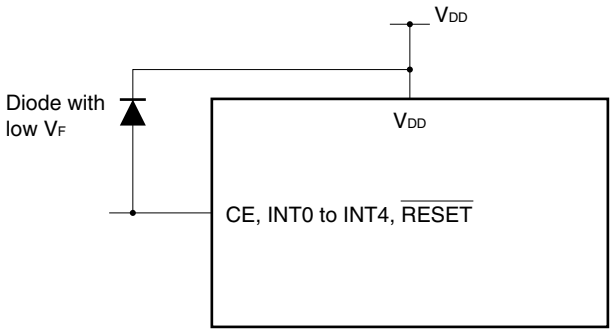
The CE, INT0 to INT4, and $\overline{\text{RESET}}$ pins have a function to set a test mode in which the internal operations of the μPD17P709A are tested (IC test), in addition to the functions listed in **1.1 Pin Function List**.

When a voltage exceeding V_{DD} is applied to any of these pins, the device is set in the test mode. If a noise exceeding V_{DD} is superimposed during normal operation, therefore, the test mode is set by mistake, affecting the normal operation.

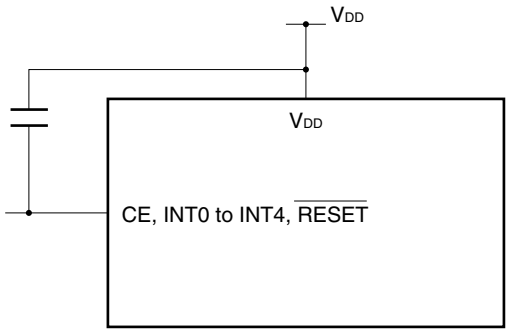
Especially if the wiring length of pins is too long, noise is superimposed on these pins. In consequence, the above problem occurs.

Therefore, keep the wiring length as short as possible to prevent noise from being superimposed. If superimposition of noise is unavoidable, connect an external component as illustrated below to suppress the noise.

- **Connect a diode with a low V_F between the pin and V_{DD}.**



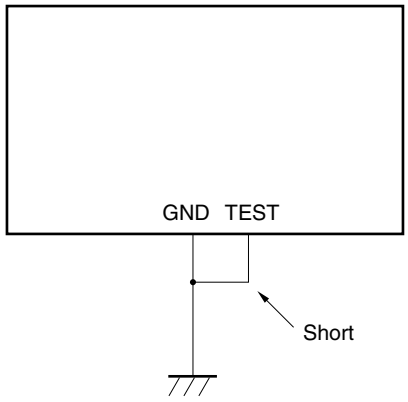
- **Connect a capacitor between the pin and V_{DD}.**



1.6 Cautions on Using TEST Pin (Only in Normal Operation Mode)

When V_{DD} is applied to the TEST pin, the device is set in the test mode or program memory write/verify mode. Therefore, be sure to keep the wiring length of this pin as short as possible, and directly connect it to the GND pin.

If the wiring length between the TEST pin and GND pin is too long, or if external noise is superimposed on the TEST pin, generating a potential difference between the TEST pin and GND pin, your program may not run normally.



2. ONE-TIME PROM (PROGRAM MEMORY) WRITE, READ, AND VERIFY

The μPD17P709A includes a 16,384 × 16-bit one-time PROM program memory. In normal operation, this PROM is accessed in 16-bit word units. During program memory write, read, and verify, the PROM is accessed in 8-bit word units. The higher 8 bits of a 16-bit word are located at an even-numbered address, and the lower 8 bits are located at an odd-numbered address.

The pins used for the write, read, and verify operations of this one-time PROM are listed in Table 2-1.

Clock input from the CLK pin, instead of address input, is used for updating addresses.

Table 2-1. Pins Used for Program Memory Write, Read, and Verify

Pin Name	Function
V_{PP}	Program voltage application (+12.5 V)
CLK	Address update clock input
MD0 to MD3	Operation mode selection
D0 to D7	8-bit data I/O
$V_{DD}0$, $V_{DD}1$	Supply voltage application (+6 V)

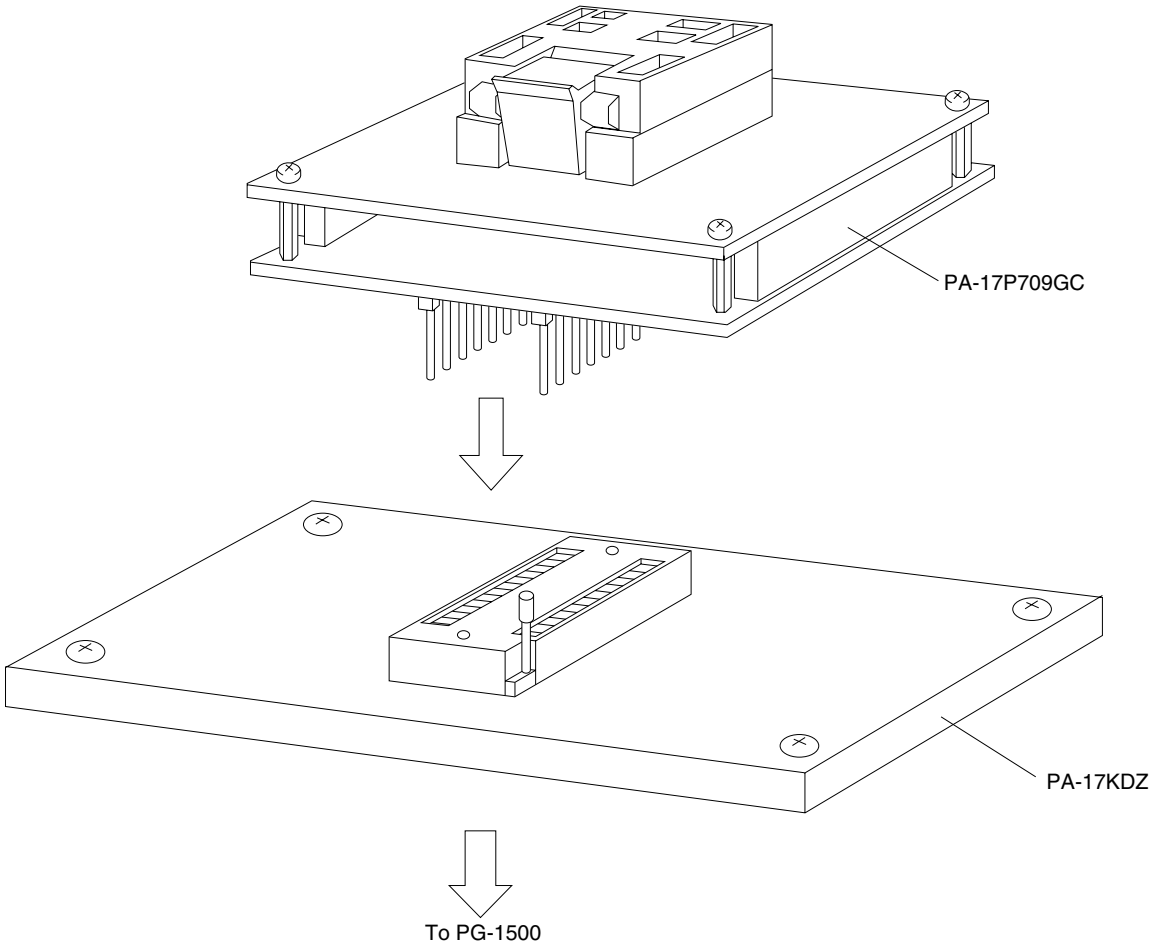
The specified PROM programmer and a dedicated programmer adapter are used for writing to the on-chip PROM.

The following PROM programmers and programmer adapters are usable.

PROM Programmer	Programmer Adapter
PG-1500 + PA-17KDZ (adapter for PG-1500)	PA17P709GC

Third-party PROM programmers are also available, such as the AF-9703, AF-9704, AF-9705, and AF-9706 (manufactured by Ando Electric Co., Ltd.)

Figure 2-1. PA-17P709GC and PA-17KDZ



2.1 Operation Modes for Program Memory Write, Read, and Verify

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD17P709A enters the program memory write, read, and verify mode.

The following operation modes can be set by setting pins MD0 to MD3 as shown below.

Pins not listed in Table 2-2 should be connected to GND via a pull-down resistor (470 Ω) (refer to **PIN CONFIGURATION (2) PROM programming mode**).

Table 2-2. Operation Mode Setting for Program Memory Write, Read, and Verify

Operation Mode Setting						Operation Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0-clear mode
		L	H	H	H	Write mode
		L	L	H	H	Write/verify mode
		H	×	H	H	Program inhibit mode

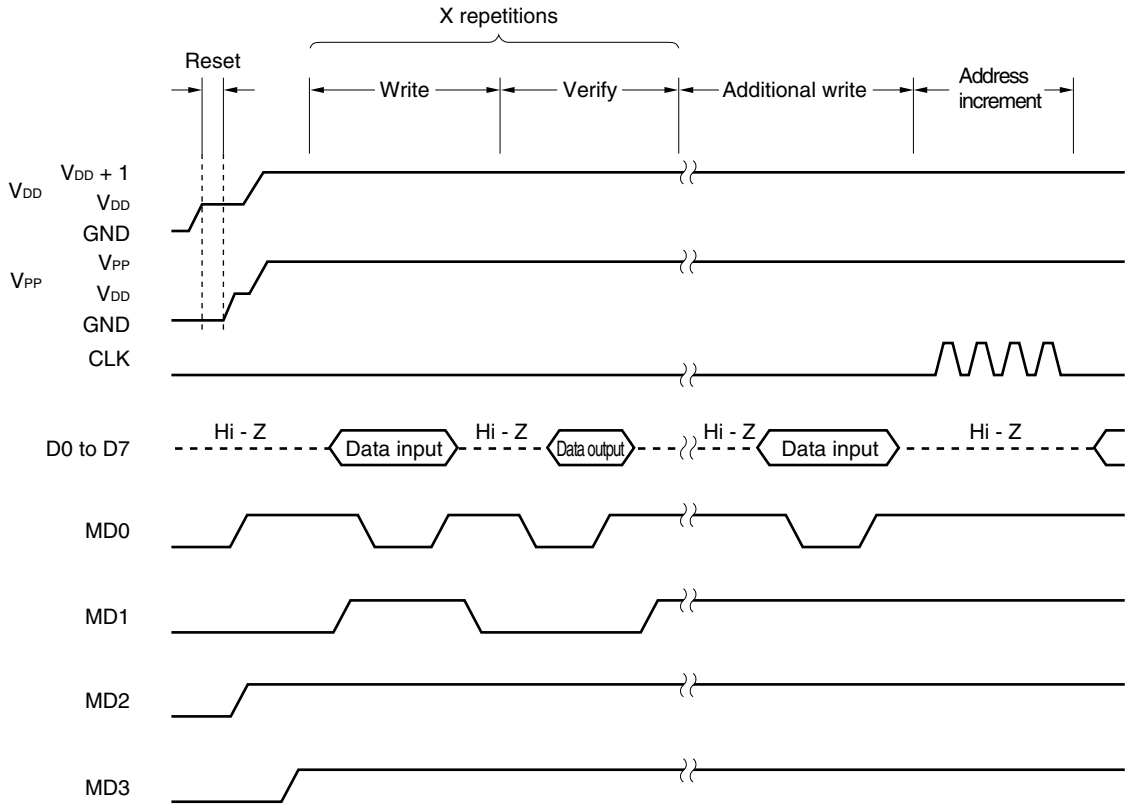
Remark ×: L or H

2.2 Program Memory Write Procedure

Program memory can be written at high speed using the following procedure.

(1) Pull down unused pins to GND via a resistor. Set the CLK pin to low.
(2) Supply 5 V to the V_{DD} pin. Set the V_{PP} pin to low.
(3) Wait for 10 μs and then supply 5 V to the V_{PP} pin.
(4) Set the mode setting pin to program memory address 0-clear mode.
(5) Supply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(6) Set the program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Set the program inhibit mode.
(9) Set the verify mode. If the data is correct, go to step (10). If not, repeat steps (7) to (9).
(10) (X: Number of write operations from steps (7) to (9)) × 1 ms additional write.
(11) Set the program inhibit mode.
(12) Input four pulses to the CLK pin to increment the program memory address by one.
(13) Repeat steps (7) to (12) until the end address is reached.
(14) Set the program memory address 0-clear mode.
(15) Change the V_{DD} and V_{PP} pins to 5 V.
(16) Turn off the power.

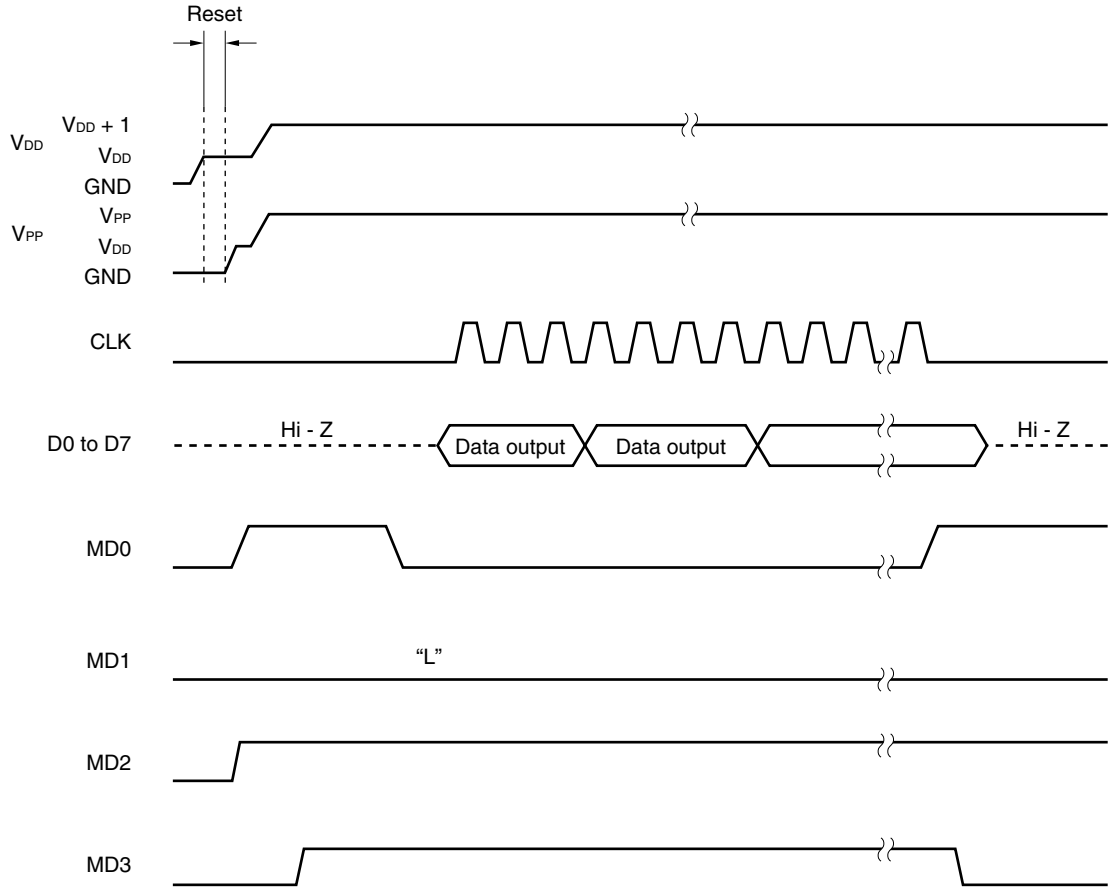
The following figure shows steps (2) to (12).



2.3 Program Memory Read Procedure

(1) Pull down unused pins to GND via a resistor. Set the CLK pin to low.
(2) Supply 5 V to the V_{DD} pin. Set the V_{PP} pin to low.
(3) Wait for 10 μs and then supply 5 V to the V_{PP} pin.
(4) Set the mode setting pin to program memory address 0-clear mode.
(5) Supply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(6) Set the program inhibit mode.
(7) Set the verify mode. Addresses are incremented by one for each 4-pulse cycle input to the CLK pin.
(8) Set the program inhibit mode.
(9) Set the program memory address 0-clear mode.
(10) Change the V_{DD} and V_{PP} pins to 5 V.
(11) Turn off the power.

The following figure shows steps (2) to (9).



3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.0	V
PROM program voltage	V_{PP}		–0.3 to +13.5	V
Input voltage	V_I	Other than CE, INT0 to INT4, and $\overline{\text{RESET}}$ pins	–0.3 to V_{DD} + 0.3	V
		CE, INT0 to INT4, and $\overline{\text{RESET}}$ pins	–0.3 to V_{DD} + 0.6	V
Output voltage	V_O	Except P1B0 to P1B3	–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–8.0	mA
		Total of P2A0 to P2A2, P3A0 to P3A3, and P3B0 to P3B3	–15.0	mA
		Total of P0A0 to P0A3, P0B0 to P0B3, P0C0 to P0C3, P1D0 to P1D3, P2B0 to P2B3, P2C0 to P2C3, P2D0 to P2D2, P3C0 to P3C3, and P3D0 to P3D3	–25.0	mA
Output current, low	I_{OL}	Per pin for P1B0 to P1B3	12.0	mA
		Per pin for P1B0 to P1B3	8.0	mA
		Total of P2A0 to P2A2, P3A0 to P3A3, and P3B0 to P3B3	15.0	mA
		Total of P0A0 to P0A3, P0B0 to P0B3, P0C0 to P0C3, P1D0 to P1D3, P2B0 to P2B3, P2C0 to P2C3, P2D0 to P2D2, P3C0 to P3C3, and P3D0 to P3D3	25.0	mA
		Total of P1B0 to P1B3 pins	25.0	mA
Output voltage	V_{BDS}	P1B0 to P1B3	14.0	V
Total power dissipation	P_t		200	mW
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	When CPU and PLL are operating	4.5	5.0	5.5	V
	V_{DD2}	When CPU and PLL are stopped	3.5	5.0	5.5	V

Recommended Output Withstanding Voltage (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output withstanding voltage	V_{BDS}	P1B0 to P1B3			12	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	When CPU is operating and PLL is stopped with sine wave input to X_{IN} pin. (f_{IN} = 4.5 MHz ±1%, V_{IN} = V_{DD})		1.5	3.0	mA
	I_{DD2}	When CPU and PLL are stopped with sine-wave input to X_{IN} pin. (f_{IN} = 4.5 MHz ±1%, V_{IN} = V_{DD}) With HALT instruction		0.7	1.5	mA
Data retention voltage	V_{DDR1}	Crystal oscillation	3.5		5.5	V
	V_{DDR2}	Crystal oscillation stopped — Power failure detection by timer FF	2.2		5.5	V
	V_{DDR3}	Crystal oscillation stopped — Data memory retained	2.0		5.5	V
Data retention current	I_{DDR1}	Crystal oscillation stopped — V_{DD} = 5 V, T_A = 25°C		2.0	4.0	μA
	I_{DDR2}	Crystal oscillation stopped		2.0	30.0	μA
Input voltage, high	V_{IH1}	P0A0, P0B1, P0C0 to P0C3, P1A0, P1A1, P1C0 to P1C3, P1D0 to P1D3, P2A2, P2B0 to P2B3, P2C0 to P2C3, P2D0 to P2D2, P3A0 to P3A3, P3B0 to P3B3, P3C0 to P3C3, P3D0 to P3D3	0.7V_{DD}		V_{DD}	V
	V_{IH2}	P0A1 to P0A3, P0B0, P0B2, P0B3, P2A0, P2A1, CE, INT0 to INT4, $\overline{\text{RESET}}$	0.8V_{DD}		V_{DD}	V
	V_{IH3}	P0D0 to P0D3	0.55V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P0A0, P0B1, P0C0 to P0C3, P1A0, P1A1, P1C0 to P1C3, P1D0 to P1D3, P2A2, P2B0 to P2B3, P2C0 to P2C3, P2D0 to P2D2, P3A0 to P3A3, P3B0 to P3B3, P3C0 to P3C3, P3D0 to P3D3	0		0.3V_{DD}	V
	V_{IL2}	P0A1 to P0A3, P0B0, P0B2, P0B3, P2A0, P2A1, CE, INT0 to INT4, $\overline{\text{RESET}}$	0		0.2V_{DD}	V
	V_{IL3}	P0D0 to P0D3	0		0.15V_{DD}	V
Output current, high	I_{OH1}	P0A0 to P0A3, P0B0 to P0B3, P0C0 to P0C3, P1D0 to P1D3, P2A0 to P2A2, P2B0 to P2B3, P2C0 to P2C3, P2D0 to P2D2, P3A0 to P3A3, P3B0 to P3B3, P3C0 to P3C3, P3D0 to P3D3 V_{OH} = V_{DD} – 1 V	–1.0			mA
	I_{OH2}	EO0, EO1 V_{DD} = 4.5 to 5.5 V, V_{OH} = V_{DD} – 1 V	–3.0			mA
Output current, low	I_{OL1}	P0A0 to P0A3, P0B0 to P0B3, P0C0 to P0C3, P1D0 to P1D3, P2A0 to P2A2, P2B0 to P2B3, P2C0 to P2C3, P2D0 to P2D2, P3A0 to PA3A, P3B0 to P3B3, P3C0 to P3C3, P3D0 to P3D3 V_{OL} = 1 V	1.0			mA
	I_{OL2}	EO0, EO1 V_{DD} = 4.5 to 5.5 V, V_{OL} = 1 V	3.0			mA
	I_{OL3}	P1B0 to P1B3 V_{OL} = 1 V	7.0			mA
Input current, high	I_{IH}	P0D0 to P0D3 pulled down V_{IN} = V_{DD}	5.0		150	μA
Output off leakage current	I_{LO1}	P1B0 to P1B3 V_{IN} = 12 V			1.0	μA
	I_{LO2}	EO0, EO1 V_{IN} = V_{DD}, V_{IN} = 0 V			±1.0	μA
Input leakage current, high	I_{LIH}	Input pin V_{IN} = V_{DD}			1.0	μA
Input leakage current, low	I_{LIL}	Input pin V_{IN} = 0 V			–1.0	μA

AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN1}	VCOL pin, MF mode	Sine-wave input V_{IN} = 0.15V_{p-p}	0.8		3	MHz
			Sine-wave input V_{IN} = 0.1V_{p-p}	0.5		3	MHz
	f_{IN2}	VCOL pin, HF mode, sine-wave input V_{IN} = 0.1V_{p-p} Note		10		40	MHz
	f_{IN3}	VCOH pin, VHF mode, sine-wave input V_{IN} = 0.1V_{p-p} Note		60		130	MHz
	f_{IN4}	AMIFC pin, sine-wave input V_{IN} = 0.15V_{p-p}		0.4		0.5	MHz
	f_{IN5}	FMIFC pin, FMIF count mode, sine-wave input V_{IN} = 0.20V_{p-p}		10		11	MHz
	f_{IN6}	FMIFC pin, AMIF count mode, sine-wave input V_{IN} = 0.15V_{p-p}		0.4		0.5	MHz
SIO0 input frequency	f_{IN7}	External clock				1	MHz
SIO1 input frequency	f_{IN8}	External clock				0.7	MHz

Note The condition of sine-wave input V_{IN} = 0.1V_{p-p} is the rated value when the μPD17P709A is operating alone. Where influence of noise must be taken into consideration, operation under input amplitude conditions of V_{IN} = 0.15V_{p-p} is recommended.

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A/D conversion total error		8 bits			±3.0	LSB
A/D conversion total error		8 bits T_A = 0 to 85°C			±2.5	LSB

Reference Characteristics (T_A = +25°C, V_{DD} = 5.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD3}	When CPU and PLL are operating with sine-wave input to VCOH pin (f_{IN} = 130 MHz, V_{IN} = 0.3V_{p-p})		6.0	12.0	mA

DC Programming Characteristics (T_A = 25°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins other than CLK	0.7V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than CLK	0		0.2V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage, high	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	I_{OL} = 1 mA			1.0	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Ensure that V_{PP} does not exceed +13.5 V including overshoot.

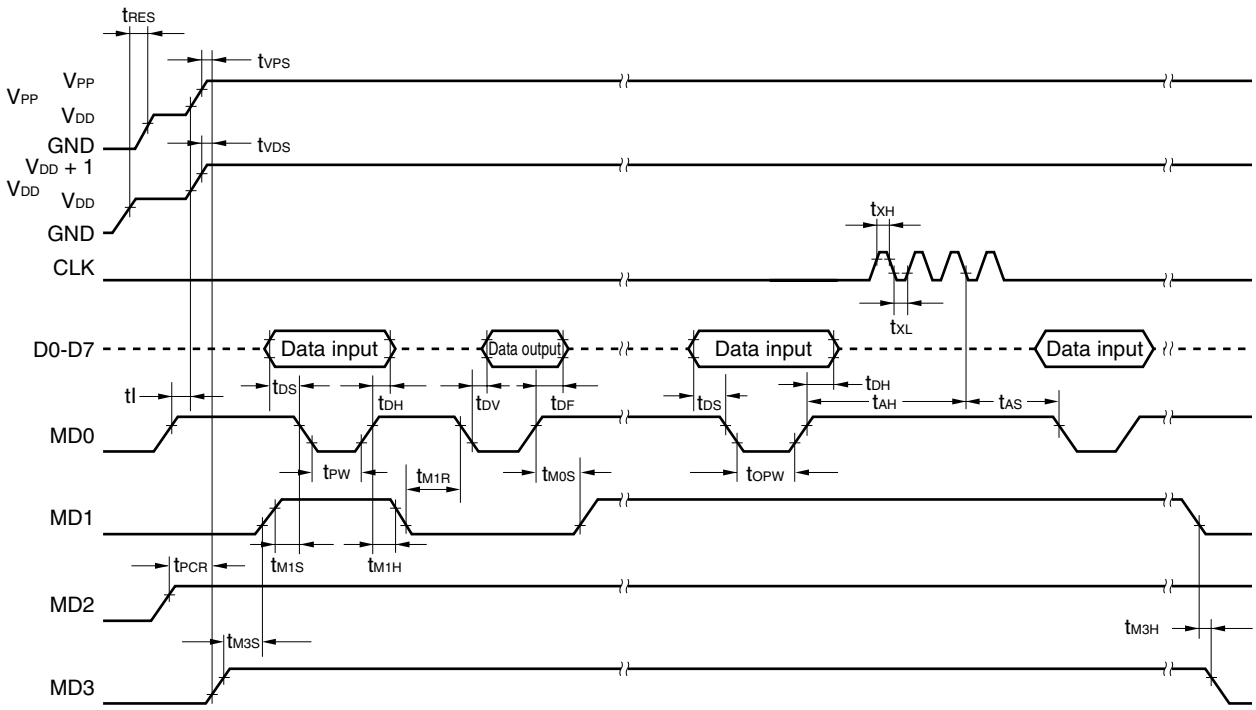
2. V_{DD} must be applied before V_{PP}, and cut after V_{PP}.

AC Programming Characteristics (T_A = 25°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time[Note] (to MD0↓)	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{M1S}		2			μs
Data setup time (to MD0↓)	t_{DS}		2			μs
Address hold time[Note] (from MD0↑)	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}		2			μs
Delay time from MD0↑ to data output float	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}		2			μs
Initial program pulse width	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{M0S}		2			μs
Delay time from MD0↓ to data output	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 recovery time (from MD0↓)	t_{M1R}		2			μs
Program counter reset time	t_{PCR}		10			μs
CLK input high-/low-level widths	t_{XH}, t_{XL}		0.125			μs
CLK input frequency	f_X				4.19	MHz
Initial mode setting time	t_I		2			μs
MD3 setup time (to MD1↑)	t_{M3S}		2			μs
MD3 hold time (from MD1↓)	t_{M3H}		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	Program memory read	2			μs
Delay time from address[Note] to data output	t_{DAD}	Program memory read			2	μs
Hold time from address[Note] to data output	t_{HAD}	Program memory read	0		130	ns
MD3 hold time (from MD0↑)	t_{M3HR}	Program memory read	2			μs
Delay time from MD3↓ to data output float	t_{DFR}	Program memory read			2	μs
Reset setup time	t_{RES}		10			μs

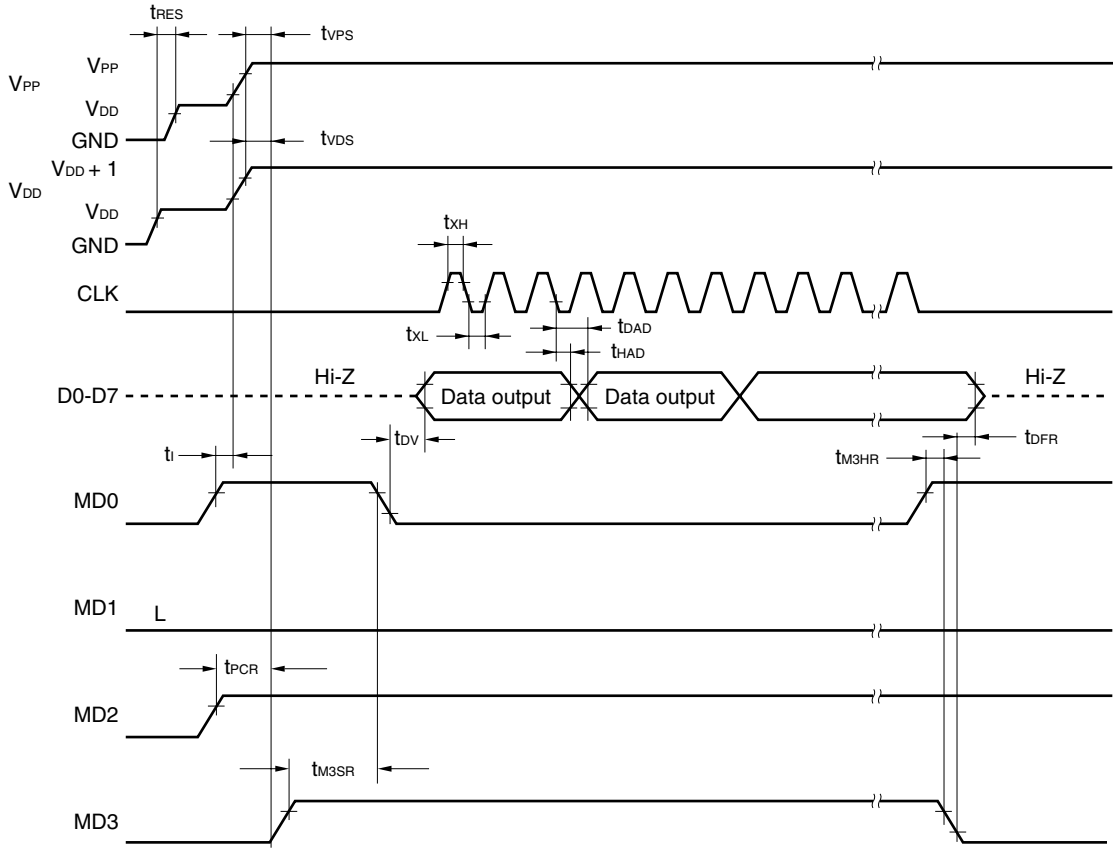
Note The internal address signal is incremented by 1 on the 3rd fall of a four-clock input (CLK) cycle, and is not connected to a pin.

Program Memory Write Timing



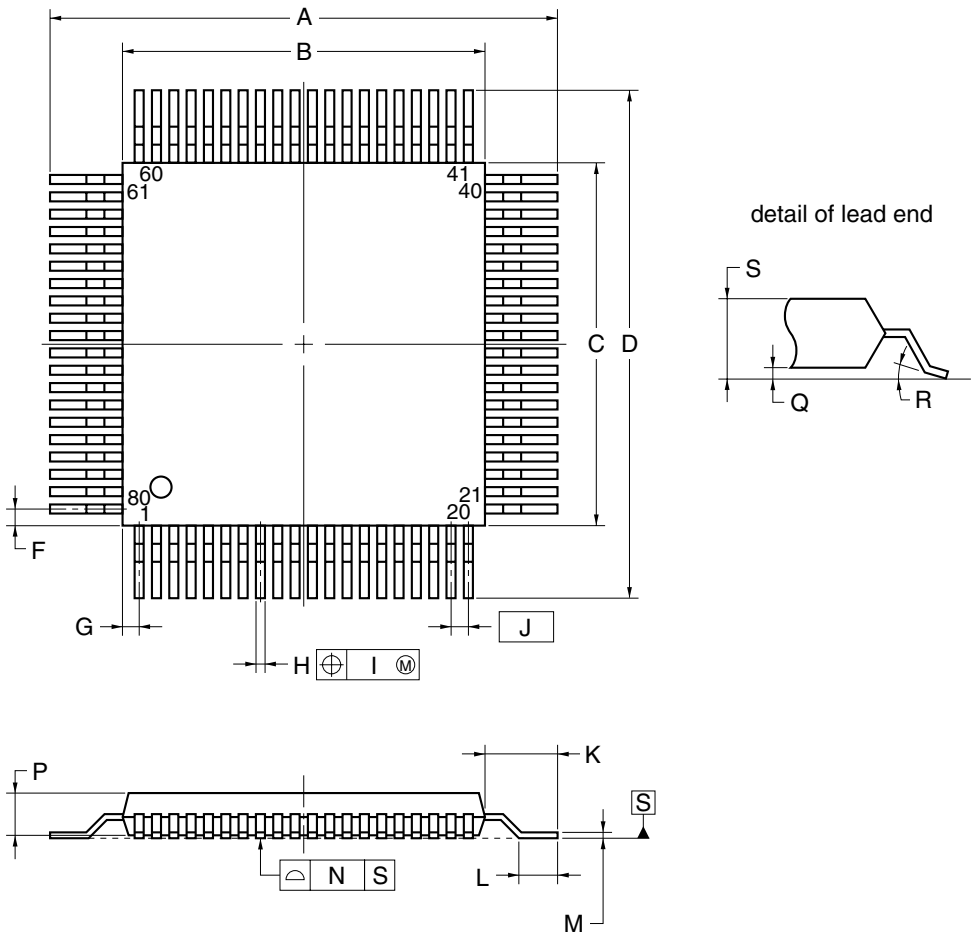
Remark The dashed line indicates high-impedance.

Program Memory Read Timing



4. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.2±0.4
B	14.0±0.2
C	14.0±0.2
D	17.2±0.4
F	0.825
G	0.825
H	0.30±0.10
I	0.13
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

S80GC-65-3B9-6

5. RECOMMENDED SOLDERING CONDITIONS

The μPD17P709A should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 5-1. Surface Mounting Type Soldering Conditions

μPD17P709AGC-3B9: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds MAX. (at 210°C or higher.), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds MAX. (at 200°C or higher.), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C MAX., Time: 10 seconds MAX., Count: Once, Preheating temperature: 120°C MAX. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C MAX., Time: 3 seconds MAX. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX DEVELOPMENT TOOLS

The following development tools are available for development of programs for the μPD17P709A.

Hardware

Name	Outline
In-circuit emulator (IE-17K-ET[Note 1])	IE-17K-ET is an in-circuit emulator that can be used with any model in the 17K Series. IE-17K-ET is connected to a host machine, which is PC-9800 series or IBM PC/AT™, with RS-232C. By using these in-circuit emulators with a system evaluation board (SE board) corresponding to each model, these emulators operate as emulators specific to a model. When man-machine interface software *SIMPLEHOST*™ is used, a more sophisticated debugging environment can be created.
SE board (SE-17709)	SE-17709 is an SE board for the μPD17709A Subseries. This board can be used alone to evaluate a system, or in combination with an in-circuit emulator for debugging.
Emulation probe (EP-17K80GC)	EP-17K80GC is an emulation probe for the μPD17P709AGC. By using this probe with EV-9200GC-80[Note 2], the SE board and target system are connected.
Conversion socket (EV-9200GC-80[Note 2])	EV-9200GC-80 is a conversion socket for 80-pin plastic QFP (14 × 14). It is used to connect the EP-17K80GC and target system.
PROM programmer (PG-1500)	PG-1500 is a PROM programmer supporting μPD17P709A. It can program the μPD17P709A when connected with the PG-1500 adapter PA-17KDZ and programmer adapter PA-17P709GC.
Programmer adapter (PA-17P709GC)	PA-17P709GC is an adapter to program the μPD17P709A. It is used with PG-1500.

Notes 1. External power supply type

2. One EV-9200GC-80 is supplied with the EP-17K80GC. Five EV-9200GC-80 are also available as a set.

Remark Third-party PROM programmers AF-9703, AF-9704, AF-9705, and AF-9706 are available from Ando Electric Co., Ltd. Use these programmers with programmer adapter PA-17P709GC. For details, consult Ando Electric Co., Ltd. (TEL: +8-44-549-7300).

Software

Name	Outline	Host Machine	OS	Media	Parts Number
17K Series assembler (RA17K)	RA17K is an assembler that can be commonly used with 17K Series. To develop programs for the μPD17P709A, this RA17K and a device file (AS17704) are used in combination.	PC-9800 series	Japanese Windows™	3.5” 2HD	μSAA13RA17K
		IBM PC/AT compatibles	Japanese Windows	3.5” 2HC	μSAB13RA17K
			English Windows		μSBB13RA17K
Device file (AS17704)	AS17704 is a device file for the μPD17P709A. It is used with the assembler common to the 17K Series (RA17K).	PC-9800 series	Japanese Windows	3.5” 2HD	μSAA13AS17704
		IBM PC/AT compatibles	Japanese Windows	3.5” 2HC	μSAB13AS17704
			English Windows		μSBB13AS17704
Support software (*SIMPLEHOST*)	*SIMPLEHOST* is man-machine interface software that runs on Windows when a program is developed by using an in-circuit emulator and personal computer.	PC-9800 series	Japanese Windows	3.5” 2HD	μSAA13ID17K
		IBM PC/AT compatibles	Japanese Windows	3.5” 2HC	μSAB13ID17K
			English Windows		μSBB13ID17K

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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