





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>J</sub>	PART NUMBER	PACKAGE		TOP-SIDE MARKING
–40°C to 125°C	ULN2003V12DR	16-Pin SOIC	Reel of 2500	U2003V12
	ULN2003V12PWR	16-Pin TSSOP	Reel of 2000	U2003V12

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Specified at T<sub>J</sub> = –40°C to 125°C unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
V <sub>IN</sub>	Pins IN1- IN7 to GND voltage	–0.3	5.5	V
V <sub>OUT</sub>	Pins OUT1 – OUT7 to GND voltage		20	V
V <sub>COM</sub>	Pin COM to GND voltage		20	V
I <sub>GND</sub>	Max GND-pin continuous current (100°C < T <sub>J</sub> < +125°C)		700	mA
	Max GND-pin continuous current (T <sub>J</sub> < +100°C)		1.0	A
P <sub>D</sub>	Total device power dissipation at T <sub>A</sub> = 85°C	16 Pin - SOIC	0.86	W
		16 Pin - TSSOP	0.68	W
ESD	ESD Rating – HBM		2	kV
	ESD Rating – CDM		500	V
T <sub>J</sub>	Operating virtual junction temperature	–55	150	°C
T <sub>stg</sub>	Storage temperature range	–55	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### DISSIPATION RATINGS<sup>(1)(2)</sup>

BOARD	PACKAGE	θ <sub>JC</sub>	θ <sub>JA</sub> <sup>(3)</sup>	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> < 25°C	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C	T <sub>A</sub> = 105°C
High-K	16-Pin SOIC	46°C/W	75°C/W	13.33 mW/°C	1.66 W	1.06 W	0.86 W	0.59 W
High-K	16-Pin TSSOP	49°C/W	95°C/W	10.44 mW/°C	1.31 W	0.84 W	0.68 W	0.47 W

(1) Maximum dissipation values for retaining device junction temperature of 150°C

(2) Refer to TI's design support web page at [www.ti.com/thermal](http://www.ti.com/thermal) for improving device thermal performance

(3) Operating at the absolute T<sub>J,max</sub> of 150°C can affect reliability– for higher reliability it is recommended to ensure T<sub>J</sub> < 125°C

### RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OUT</sub>	Channel off-state output pull-up voltage			16	V
V <sub>COM</sub>	COM pin voltage			16	V
I <sub>OUT(ON)</sub>	Per channel continuous sink current	V <sub>INx</sub> = 3.3V		100 <sup>(1)</sup>	mA
		V <sub>INx</sub> = 5.0V		140 <sup>(1)</sup>	
T <sub>J</sub>	Operating junction temperature	–40		125	°C

(1) 1) Refer to [ABSOLUTE MAXIMUM RATINGS](#) for T<sub>J</sub> dependent absolute maximum GND-pin current

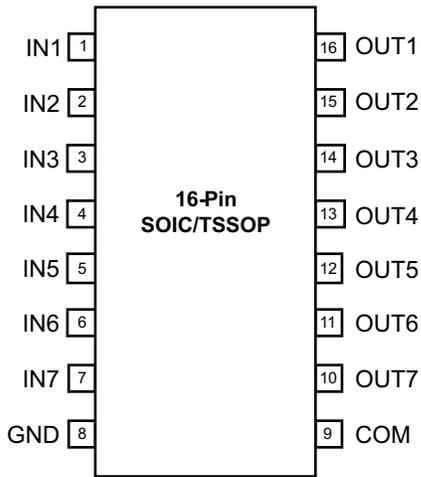
## ELECTRICAL CHARACTERISTICS

Specified over the recommended junction temperature range  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and over recommended operating conditions unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

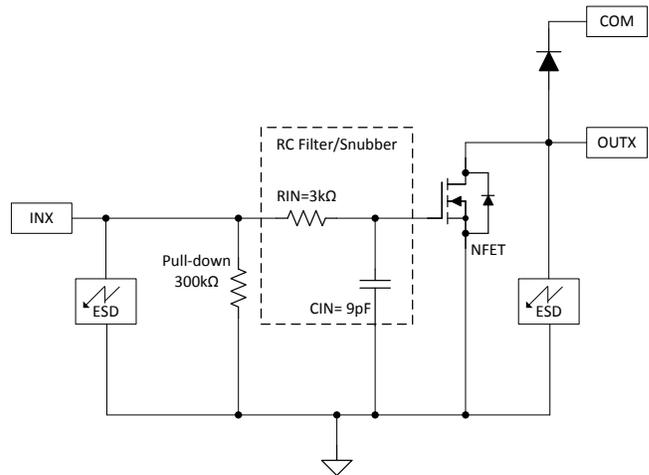
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>INPUTS IN1 THROUGH IN7 PARAMETERS</b>						
$V_{I(ON)}$	IN1–IN7 logic high input voltage	$V_{pull-up} = 3.3\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$ , $I_{OUTX} = 3.2\text{ mA}$			1.65	V
$V_{I(OFF)}$	IN1–IN7 logic low input voltage	$V_{pull-up} = 3.3\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$ , ( $I_{OUTX} < 20\text{ }\mu\text{A}$ )			0.6	
$I_{I(ON)}$	IN1–IN7 ON state input current	$V_{pull-up} = 12\text{ V}$ , $V_{INx} = 3.3\text{ V}$			12	$\mu\text{A}$
$I_{I(OFF)}$	IN1–IN7 OFF state input leakage	$V_{pull-up} = 12\text{ V}$ , $V_{INx} = 0\text{ V}$			250	nA
<b>OUTPUTS OUT1 THROUGH OUT7 PARAMETERS</b>						
$V_{OL(VCE-SAT)}$	OUT1–OUT7 low-level output voltage	$V_{INX} = 3.3\text{ V}$ , $I_{OUTX} = 20\text{ mA}$			0.12	0.15
		$V_{INX} = 3.3\text{ V}$ , $I_{OUTX} = 100\text{ mA}$			0.60	0.75
		$V_{INX} = 5.0\text{ V}$ , $I_{OUTX} = 20\text{ mA}$			0.09	0.11
		$V_{INX} = 5.0\text{ V}$ , $I_{OUTX} = 140\text{ mA}$			0.60	0.75
$I_{OUT(ON)}$	OUT1–OUT7 ON-state continuous current <sup>(1)</sup> <sup>(2)</sup> at $V_{OUTX} = 0.6\text{ V}$	$V_{INX} = 3.3\text{ V}$ , $V_{OUTX} = 0.6\text{ V}$			80	100
		$V_{INX} = 5.0\text{ V}$ , $V_{OUTX} = 0.6\text{ V}$			95	140
$I_{OUT(OFF)(ICEX)}$	OUT1–OUT7 OFF-state leakage current	$V_{INX} = 0\text{ V}$ , $V_{OUTX} = V_{COM} = 16\text{ V}$			0.5	$\mu\text{A}$
<b>SWITCHING PARAMETERS<sup>(3)(4)</sup></b>						
$t_{PHL}$	OUT1–OUT7 logic high propagation delay	$V_{INX} = 3.3\text{ V}$ , $V_{pull-up} = 12\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$			50	70
$t_{PLH}$	OUT1–OUT7 logic low propagation delay	$V_{INX} = 3.3\text{ V}$ , $V_{pull-up} = 12\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$			121	140
$t_{CHANNEL}$	Channel to Channel delay	Over recommended operating conditions and with same test conditions on channels.			15	50
$R_{PD}$	IN1–IN7 input pull-down Resistance		210k	300k	390k	$\Omega$
$\zeta$	IN1–IN7 Input filter time constant		9			ns
$C_{OUT}$	OUT1–OUT7 output capacitance	$V_{INX} = 3.3\text{ V}$ , $V_{OUTX} = 0.4\text{ V}$			15	pF
<b>FREE-WHEELING DIODE PARAMETERS<sup>(5)(4)</sup></b>						
$V_F$	Forward voltage drop	$I_{F-peak} = 140\text{ mA}$ , $V_F = V_{OUTX} - V_{COM}$			1.2	V
$I_{F-peak}$	Diode peak forward current		140			mA

- (1) The typical continuous current rating is limited by  $V_{OL} = 0.6\text{ V}$ . Whereas, absolute maximum operating continuous current may be limited by the Thermal Performance parameters listed in the Dissipation Rating Table and other Reliability parameters listed in the Recommended Operating Conditions Table.
- (2) Refer to the Absolute Maximum Ratings Table for  $T_J$  dependent absolute maximum GND-pin current.
- (3) Rise and Fall propagation delays,  $t_{PHL}$  and  $t_{PLH}$ , are measured between 50% values of the input and the corresponding output signal amplitude transition.
- (4) Guaranteed by design only. Validated during qualification. Not measured in production testing.
- (5) Not rated for continuous current operation – for higher reliability use an external freewheeling diode for inductive loads resulting in more than specified maximum free-wheeling, diode peak current across various temperature conditions

**DEVICE INFORMATION**



**Figure 1. ULN2003V12 PINOUT**



**Figure 2. Channel Block Diagram**

**ULN2003V12 PIN DESCRIPTION**

NAME	PIN NUMBER		DESCRIPTION
	16-SOIC	16-TSSOP	
IN1 – IN7	1–7	1–7	Logic Input Pins IN1 through IN7
GND	8	8	Ground Reference Pin
COM	9	9	Internal Free-Wheeling Diode Common Cathode Pin
OUT7 – OUT1	10–16	10–16	Channel Output Pins OUT7 through OUT1

## APPLICATION INFORMATION

### TTL and other Logic Inputs

ULN2003V12 input interface is specified for standard 3V and 5V CMOS logic interface. However, ULN2003V12 input interface may support other logic input levels as well. Refer to [Figure 10](#) and [Figure 11](#) to establish VOL and the corresponding typical load current levels for various input voltage ranges. Application Information section shows an implementation to drive 1.8V relays using ULN2003V12.

### Input RC Snubber

ULN2003V12 features an input RC snubber that helps prevent spurious switching in noisy environment. Connect an external 1kΩ to 5kΩ resistor in series with the input to further enhance ULN2003V12's noise tolerance.

### High-impedance Input Drivers

ULN2003V12 features a 300kΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the ULN2003V12 detects the channel input as a low level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

### On-chip Power Dissipation

Use the below equation to calculate ULN2003V12 on-chip power dissipation  $P_D$ :

$$P_D = \sum_{i=1}^N V_{OLi} \times I_{Li}$$

Where:

N is the number of channels active together.

$V_{OLi}$  is the  $OUT_i$  pin voltage for the load current  $I_{Li}$ .

(1)

### Thermal Reliability

It is recommended to limit ULN2003V12 IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate the maximum allowable on-chip power dissipation for a target IC junction temperature:

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

Where:

$T_{J(MAX)}$  is the target maximum junction temperature.

$T_A$  is the operating ambient temperature.

$\theta_{JA}$  is the package junction to ambient thermal resistance.

(2)

### Improving Package Thermal Performance

The package  $\theta_{JA}$  value under standard conditions on a High-K board is listed in the [DISSIPATION RATINGS](#).  $\theta_{JA}$  value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce  $\theta_{JA}$  and thus improve device thermal capabilities. Refer to TI's design support web page at [www.ti.com/thermal](http://www.ti.com/thermal) for a general guidance on improving device thermal performance.

## Application Examples

### Inverting Logic Level Shifter

To use ULN2003V12 as an open-collector or an open-drain inverting logic level shifter configure the device as shown in Figure 3. The ULN2003V12's each channel input and output logic levels can also be set independently. When using different channel input and output logic voltages connect the ULN2003V12 COM pin to the maximum voltage.

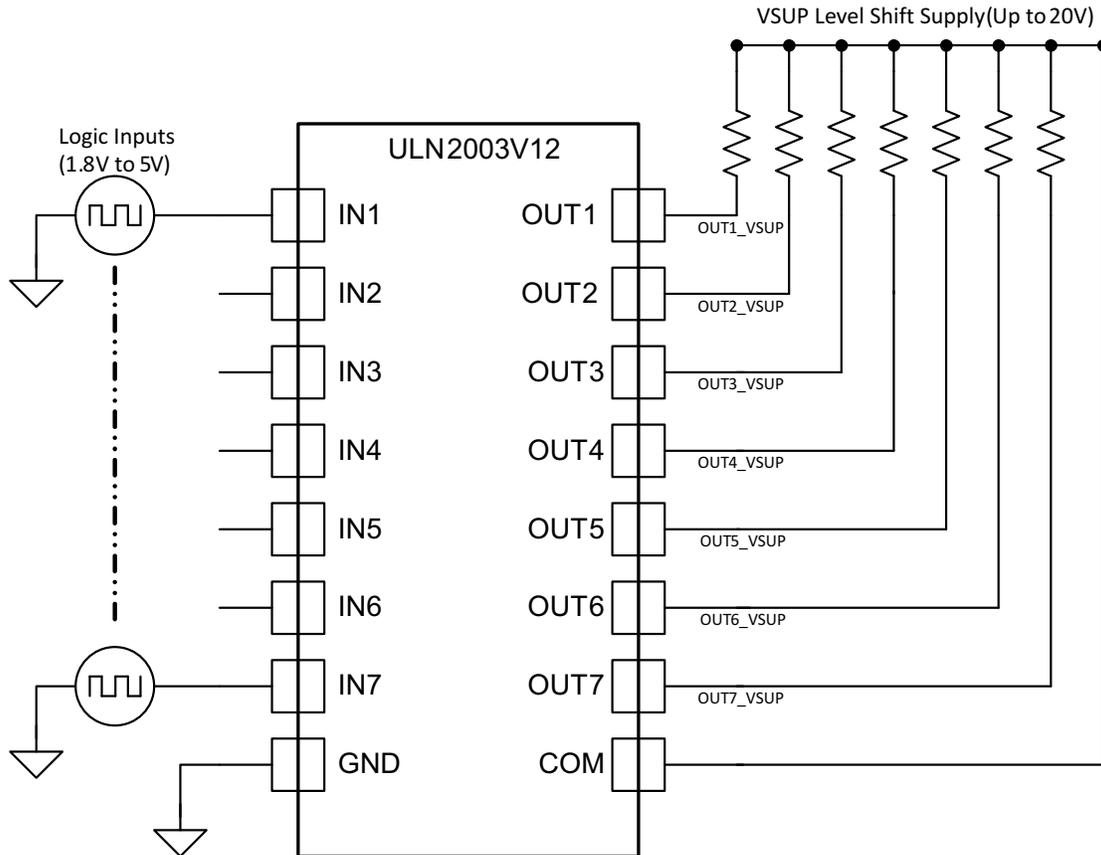


Figure 3. ULN2003V12 as Inverting Logic Level Shifter

### Max Supply Selector

Figure 4 implements a max supply selector along with a 4-channel logic level shifter using a single ULN2003V12. This setup configures ULN2003V12's channel clamp diodes OUT5 – OUT7 in a diode-OR configuration and thus the maximum supply among VSUP1, VSUP2 and VSUP3 becomes available at the COM pin. The maximum supply is then used as a pull-up voltage for level shifters. Limit the net GND pin current to less than 100mA DC to ensure reliability of the conducting diode. The unconnected inputs IN5-IN7 are pulled to GND potential through 300kΩ internal pull-down resistor.

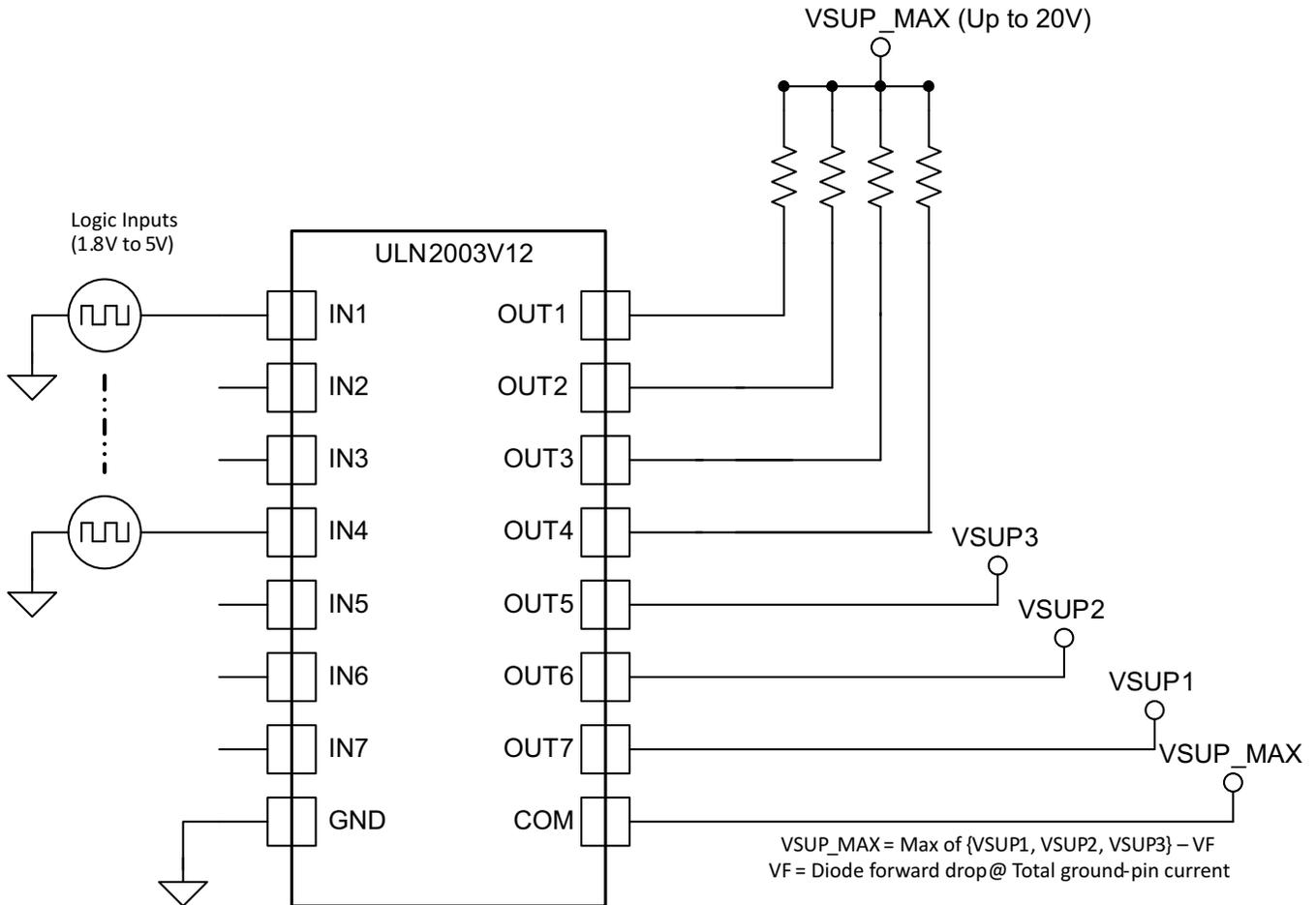
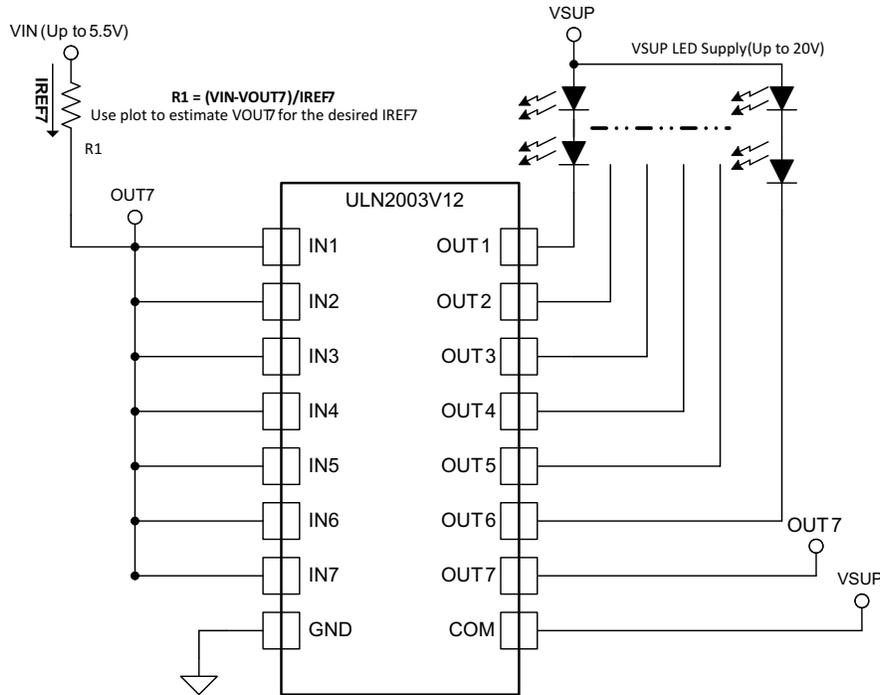


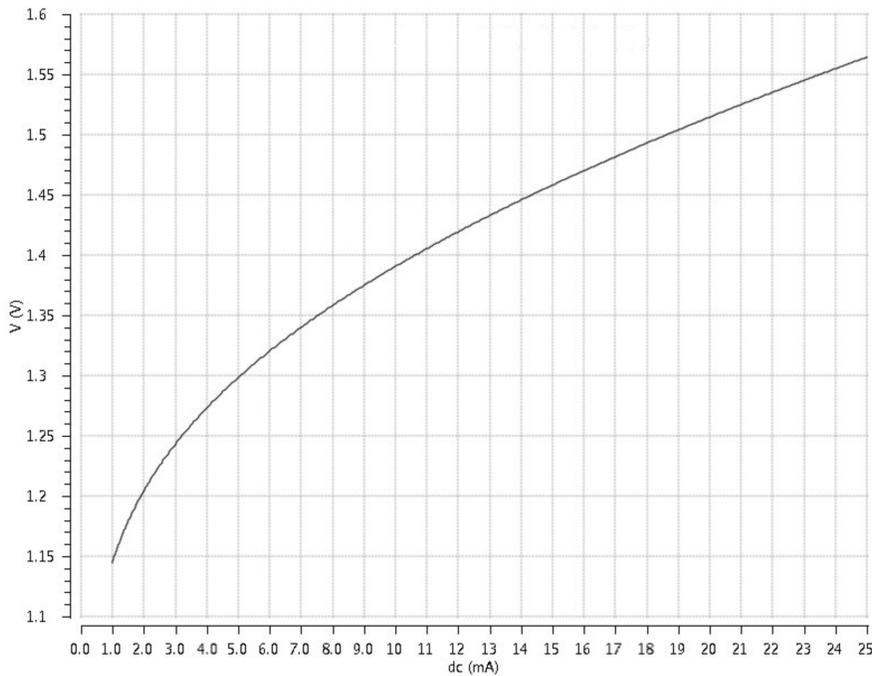
Figure 4. ULN2003V12 as Max Supply Selector

**Constant Current Generation**

When configured as per [Figure 5](#) the ULN2003V12 outputs OUT1-OUT6 act as independent constant current sources. The current flowing through the resistor R1 is copied on all other channels. To increase the current sourcing connect several output channels in parallel. To ensure best current copying set voltage drop across connected load such that VOUTx matches to VOUT7.



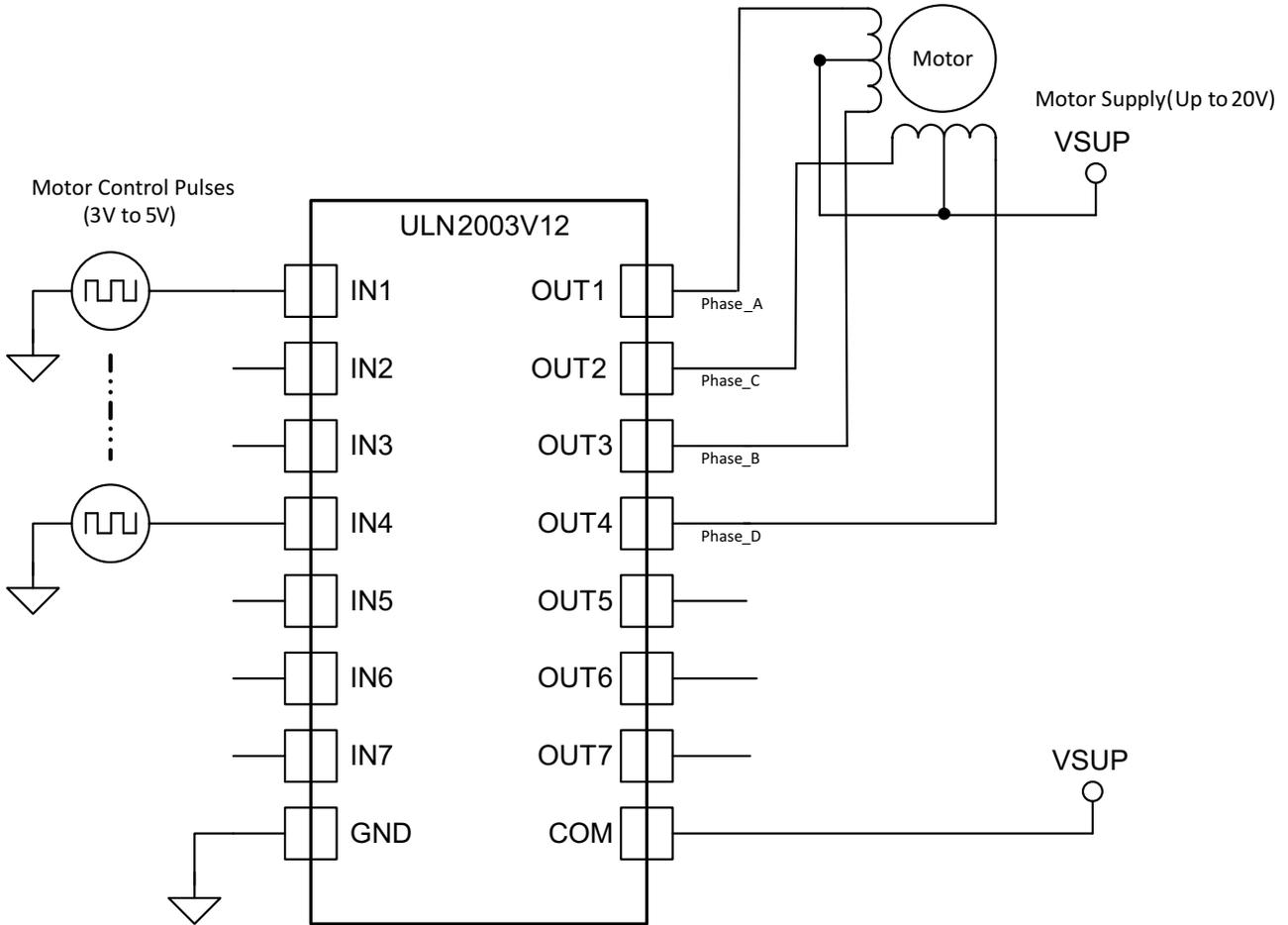
**Figure 5. ULN2003V12 as a Constant Current Driver**



**Figure 6. ULN2003V12 VOUT vs IREF**

**Unipolar Stepper Motor Driver**

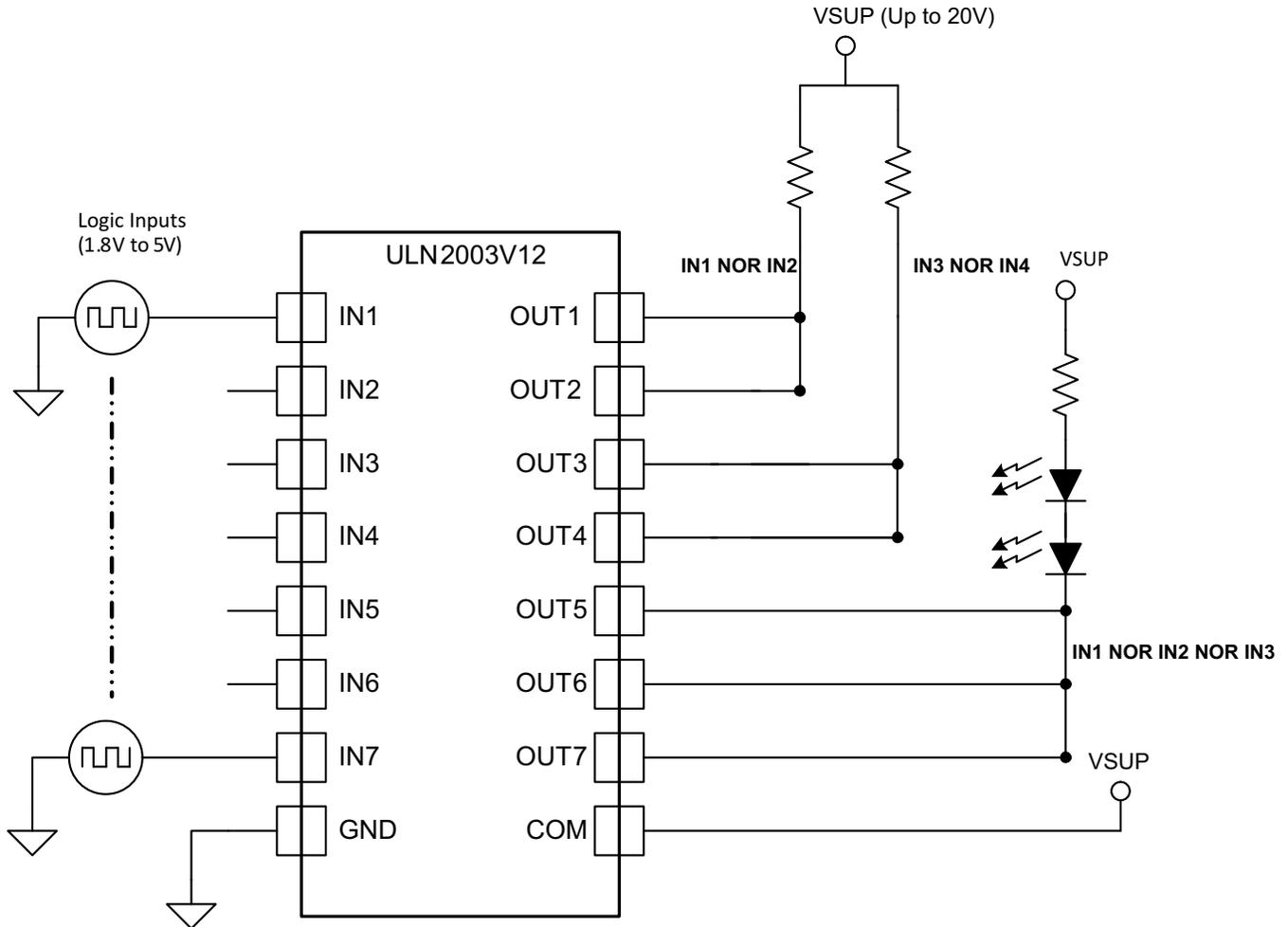
Figure 7 shows an implementation of ULN2003V12 for driving a unipolar stepper motor. The unconnected input channels can be used for other functions. When an input pin is left open the internal 300kΩ pull down resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins.



**Figure 7. ULN2003V12 as a Stepper Motor Driver**

**NOR Logic Driver**

Figure 8 shows a NOR Logic driver implementation using ULN2003V12. The output channels sharing a common pull-up resistor implement a logic NOR of the respective channel inputs. The LEDs connected to outputs OUT5-OUT7 light up when any of the inputs IN5-IN7 is logic-high (> VIH).



**Figure 8. ULN2003V12 as a NOR driver**

TYPICAL CHARACTERISTICS

T<sub>A</sub> = +25°C

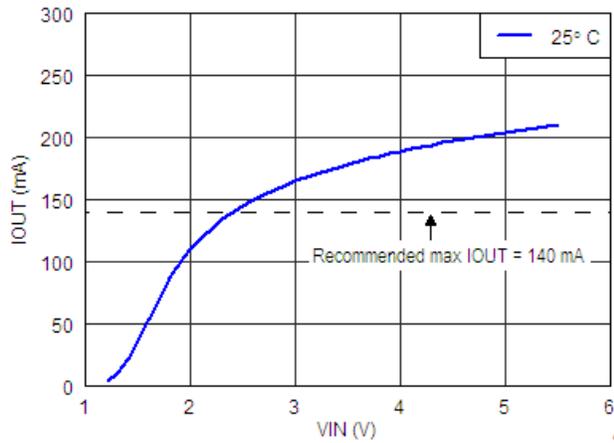


Figure 9. Load Current 1-Channel; VOL=0.6V

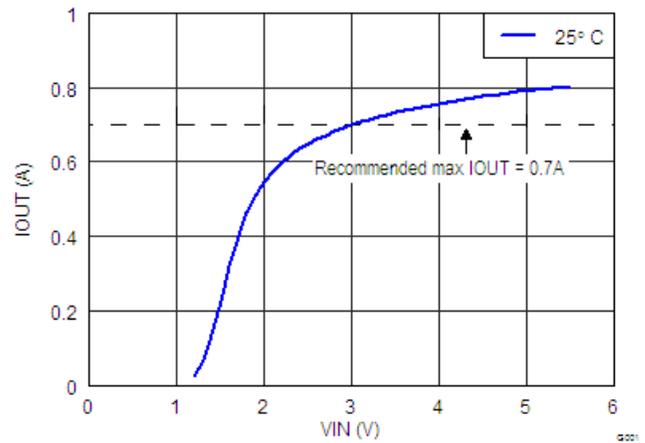


Figure 10. Load Current 7-Channels in parallel; VOL=0.6V

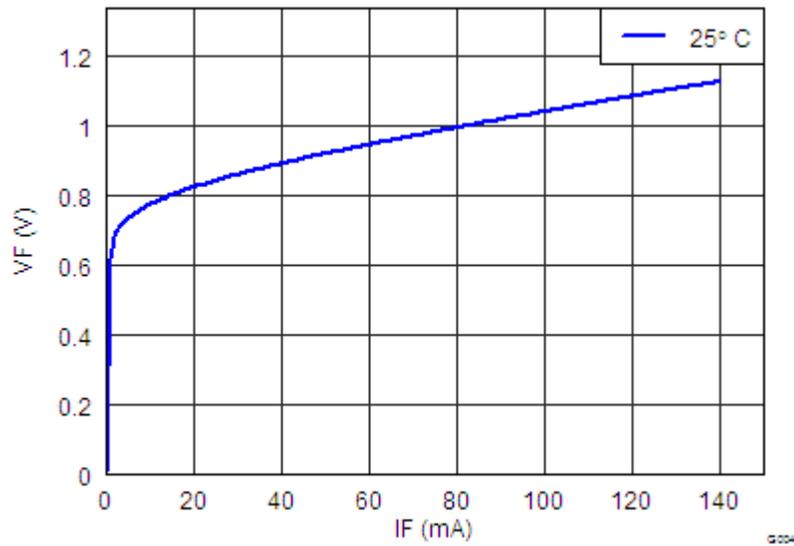
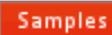


Figure 11. Freewheeling Diode VF versus IF

## REVISION HISTORY

Changes from Revision A (July 2012) to Revision B	Page
• Changed Operating Temperature Range .....	2
• Added Details to Dissipation Data .....	2
• Added Details to Switching Parameters .....	3
• Changed Detailed Block Diagram .....	4

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ULN2003V12DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	U2003V12	
ULN2003V12PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	U2003V12	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003V12PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

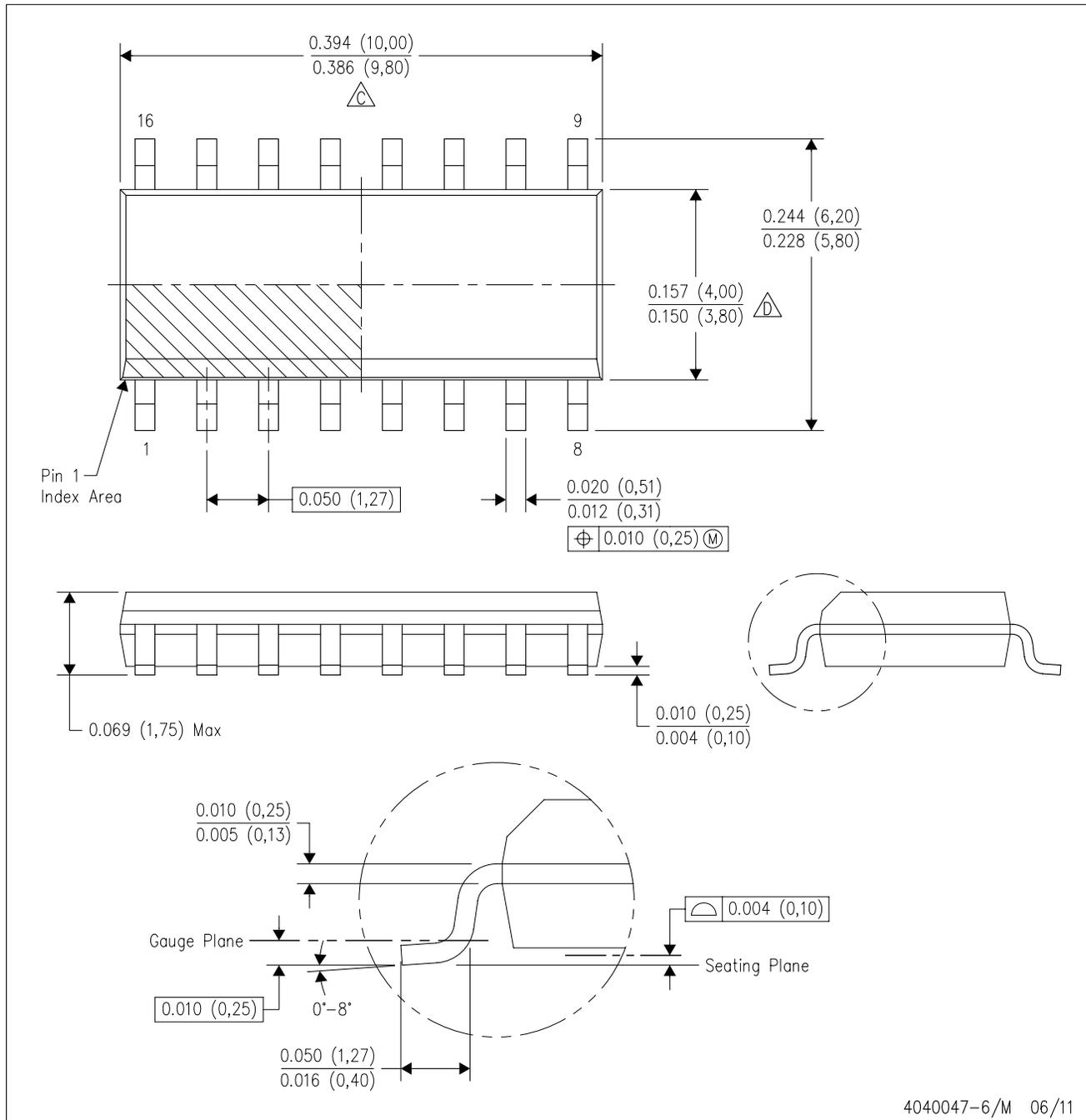


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003V12PWR	TSSOP	PW	16	2000	364.0	364.0	27.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

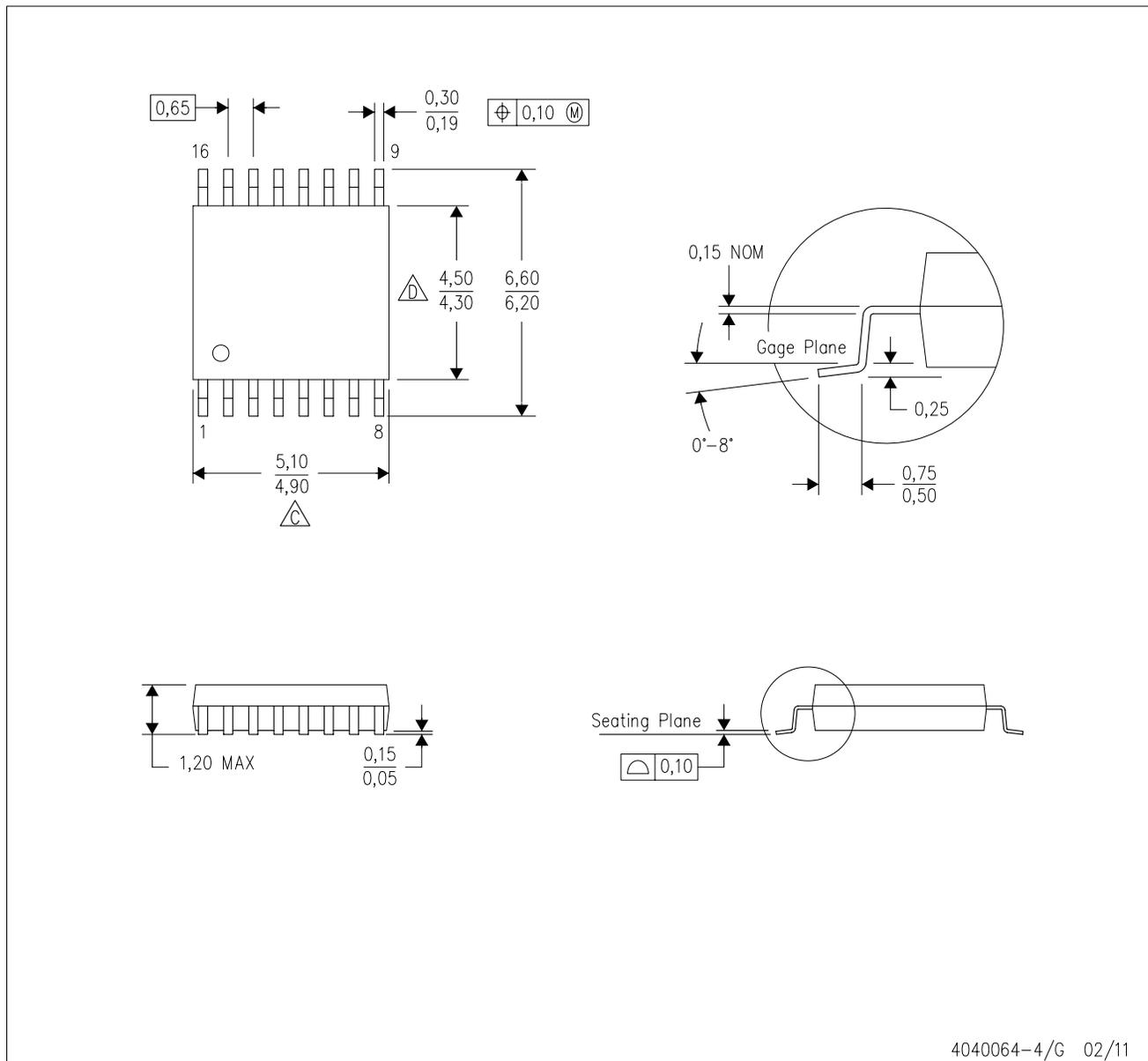


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

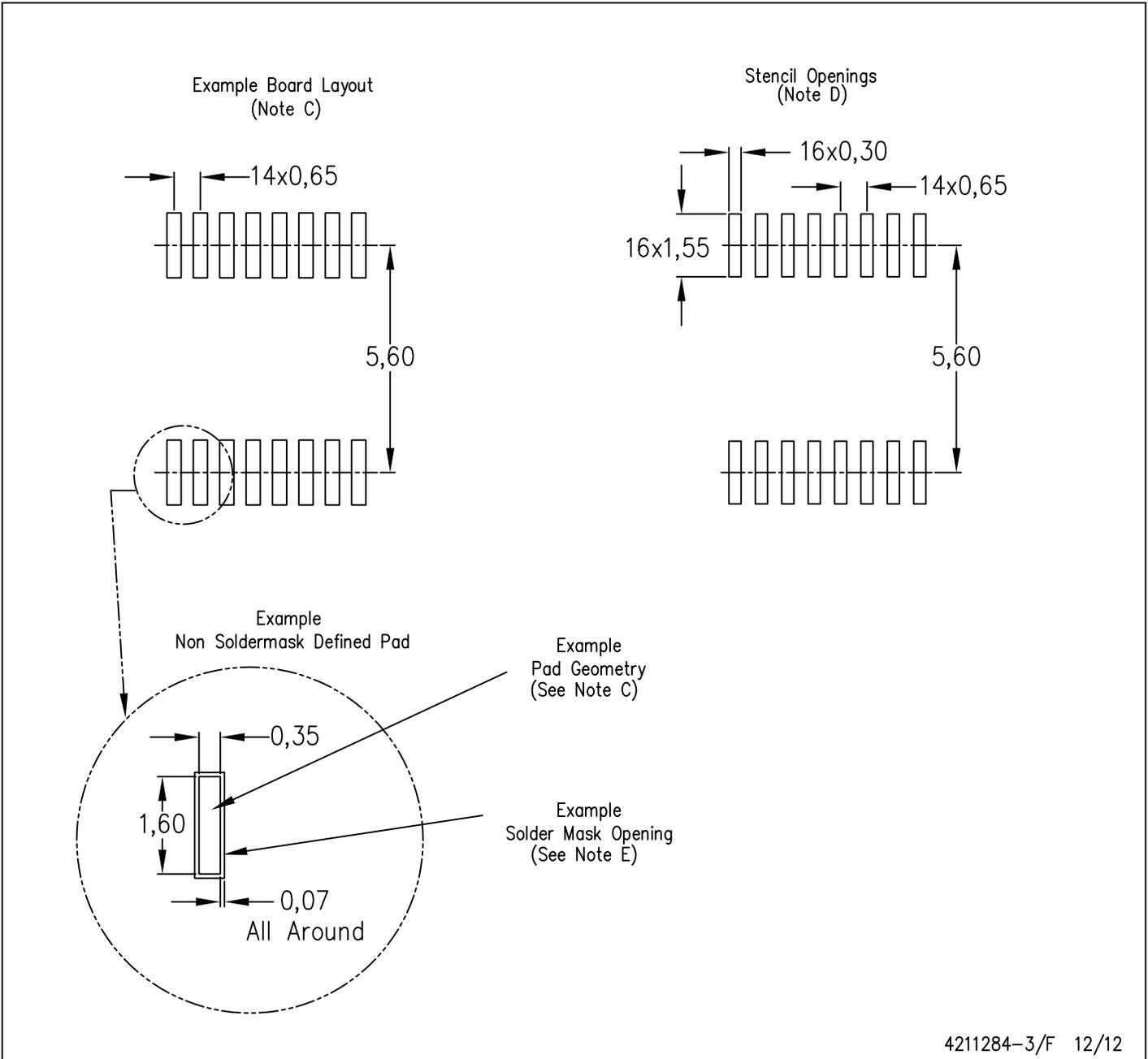


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

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Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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### Applications

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