National Semiconductor

DS3667 TRI-STATE® Bidirectional Transceiver

General Description

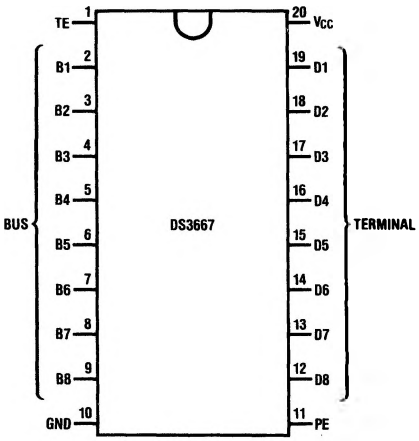
The DS3667 is a high-speed Schottky 8-channel bidirectional transceiver designed for digital information and communication systems. Pin selectable totem-pole/open collector outputs are provided at all driver outputs. This feature, together with the Dumb Mode which puts both driver and receiver outputs in TRI-STATE at the same time, means higher flexibility of system design. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. A power up/down protection circuit is included at all outputs to provide glitch-free operation during V_{CC} power up or down.

Features

- 8-channel bidirectional non-inverting transceivers
- Bidirectional control implemented with TRI-STATE output design
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- Pin selectable totem-pole/open collector outputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- Power up/down protection (glitch-free)
- Dumb Mode capability

Connection Diagram

Dual-In-Line Package



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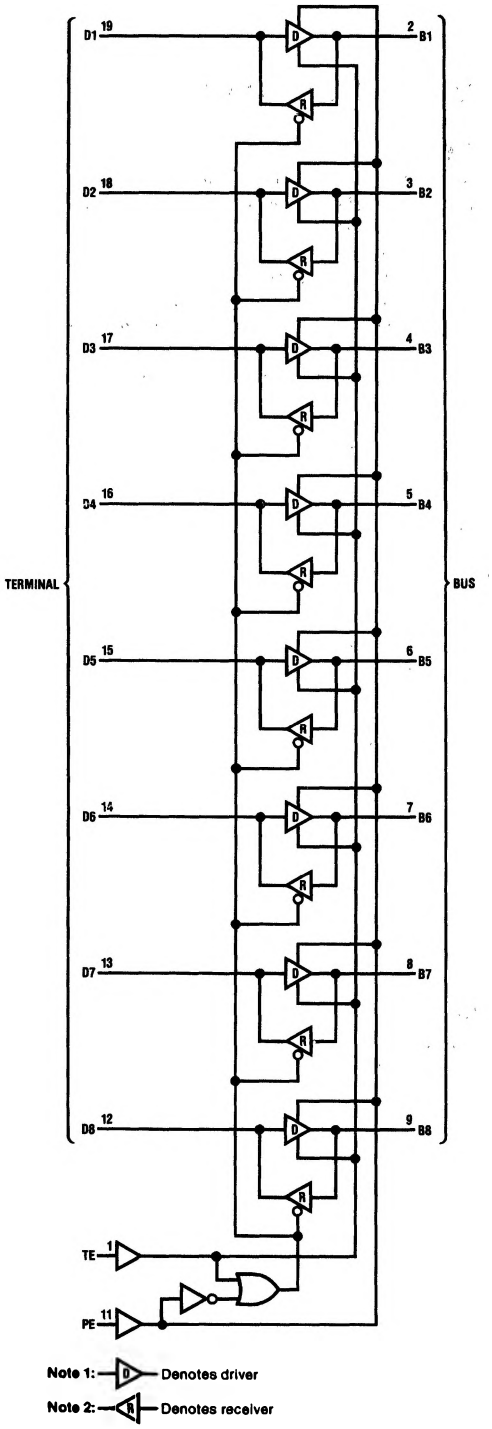
Top View

Order Number DS3667N
See NS Package Number N20A

Logic Diagram



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Functional Truth Table

Control Input Level		Data Transceivers		
TE	**PE**	**Mode**	**Bus Port**	**Terminal Port**
H	H	T	Totem-Pole Output	Input
H	L	T	Open Collector Output	Input
L	H	R	Input	Output
L	L	D	TRI-STATE	TRI-STATE

H: High Level Input
L: Low Level Input
T: Transmitting Mode
R: Receiving Mode
D: Dumb Mode

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1832 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		I_I = −18 mA		−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus		400	500		mV
V_{OH}	High Level Output Voltage	Terminal	I_{OH} = −800 μA	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA	2.5	3.4		
V_{OL}	Low Level Output Voltage	Terminal	I_{OL} = 16 mA		0.3	0.5	V
		Bus	I_{OL} = 48 mA		0.4	0.5	
I_{IH}	High Level Input Current	TE, PE	V_I = 5.5V		0.2	100	μA
			V_I = 2.7V		0.1	20	
		Terminal and Bus	V_I = 4V			200	
I_{IL}	Low Level Input Current	Terminal and TE, PE	V_I = 0.5V		−10	−100	μA
		Bus			−0.4	−1.0	mA
I_{OS}	Short Circuit Output Current	Terminal	V_I = 2V, V_O = 0V (Note 4)	−15	−35	−75	mA
		Bus		−50	−120	−200	
I_{CC}	Supply Current		Transmit, TE = 2V, PE = 2V, V_I = 0.8V		75	100	mA
			Receive, TE = 0.8V, PE = 2V, V_I = 0.8V		65	90	
C_{IN}	Bus-Port Capacitance	Bus	V_{CC} = 0V, V_I = 0V, f = 10 kHz (Note 5)		20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operations.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This parameter is guaranteed by design. It is not a tested parameter.

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C (Note 1)

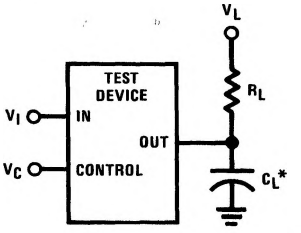
Symbol	Parameter	From	To	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	V_L = 2.3V, R_L = 38.3Ω, C_L = 30 pF *(Figure 1)*		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	V_L = 5.0V, R_L = 240Ω, C_L = 30 pF *(Figure 2)*		15	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20	ns
t_{PZH}	Output Enable Time to High Level	TE (Notes 2 and 3)	Bus	V_I = 3.0V, V_L = 0V, R_L = 480Ω, C_L = 15 pF *(Figure 1)*		19	30	ns
t_{PHZ}	Output Disable Time to High Level					15	20	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 2.3V, R_L = 38.3Ω, C_L = 15 pF *(Figure 1)*		24	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Enable Time to High Level	TE, PE (Notes 2 and 3)	Terminal	V_I = 3.0V, V_L = 0V, R_L = 3 kΩ, C_L = 15 pF *(Figure 1)*		19	35	ns
t_{PHZ}	Output Disable Time to High Level					17	25	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V, V_L = 5V, R_L = 280Ω, C_L = 15 pF *(Figure 1)*		27	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Pull-Up Enable Time	PE (Notes 2 and 3)	Bus	V_I = 3V, V_L = 0V, R_L = 480Ω, C_L = 15 pF *(Figure 1)*		10	20	ns
t_{PHZ}	Output Pull-Up Disable Time					10	20	ns

Note 1: All typical values are for T_A = 25°C, V_{CC} = 5V.

Note 2: Refer to Functional Truth Table for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations



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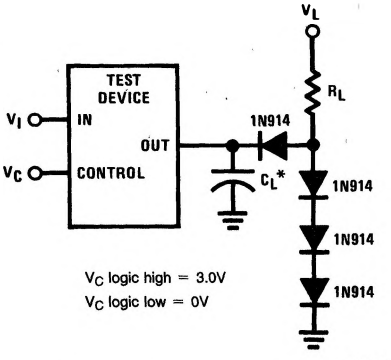
V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



V_C logic high = 3.0V
V_C logic low = 0V

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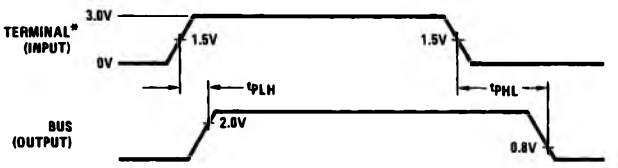
*C_L includes jig and probe capacitance

FIGURE 2

Switching Waveforms

Transmit Propagation Delays



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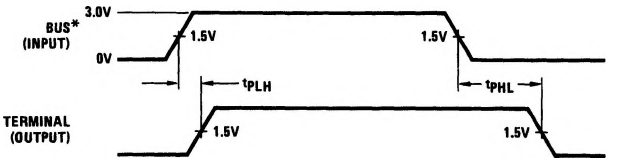
Receive Propagation Delays



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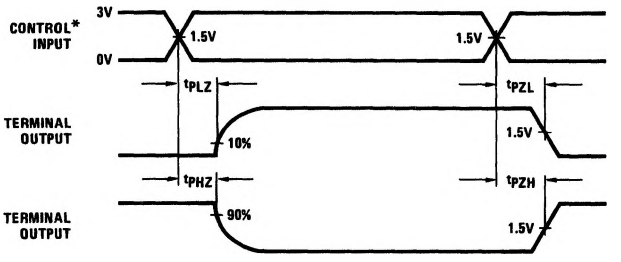
Terminal Enable/Disable Times



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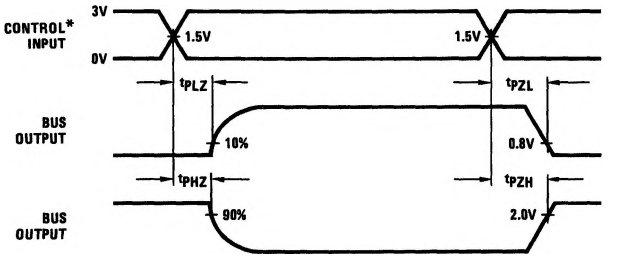
Bus Enable/Disable Times



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*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns