National Semiconductor

9334/DM9334 8-Bit Addressable Latch

General Description

The DM9334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.

The DM9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

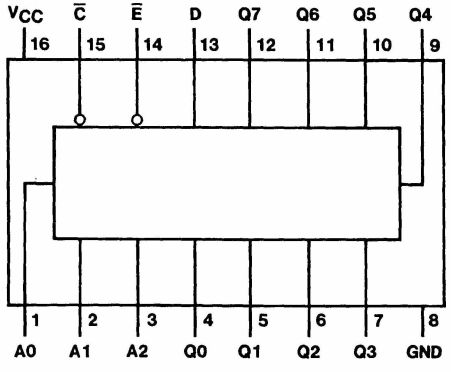
The function tables summarize the operation of the product.

Features

- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability
- Alternate Military/Aerospace device (9334) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



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Order Number 9334DMQB, 9334FMQB, DM9334J or DM9334N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0° to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	ENABLE Pulse Width (Fig. 1) (Note 4)		19	13		19	13		ns
t_{SU}	Setup Time (Note 4)	Data 1 (Fig. 4)	20	13		20	13		ns
		Data 0 (Fig. 4)	20	14		20	14		
		Address (Fig. 6) (Note 1)	10	5		10	5		
t_H	Hold Time (Note 4)	Data 1 (Fig. 4)	0	−10		0	−10		ns
		Data 0 (Fig. 4)	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	$\overline{E}$ Input			60	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	$\overline{E}$ Input			−2.4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−30		−100	mA
			COM	−30		−100	
I_{CC}	Supply Current	V_{CC} = Max			56	86	mA

Note 1: The ADDRESS setup time is the time before the negative ENABLE transition that the ADDRESS must be stable so that the correct latch is addressed without affecting the other latches.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output, Fig. 1		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output, Fig. 1		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output, Fig. 2		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output, Fig. 2		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Address to Output, Fig. 3		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Address to Output, Fig. 3		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output, Fig. 5		31	ns

Function Tables

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active High Eight Channel Demultiplexer
H	L	Clear

Inputs						Present Output States								Mode
$\overline{C}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
o	o	o		o					o					Demultiplex
o	o	o		o					o					
o	o	o		o					o					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						Addressable Latch
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

X = Don't Care Condition

L = Low Voltage Level

H = High Voltage Level

Q_{N-1} = Previous Output State

Logic Diagram

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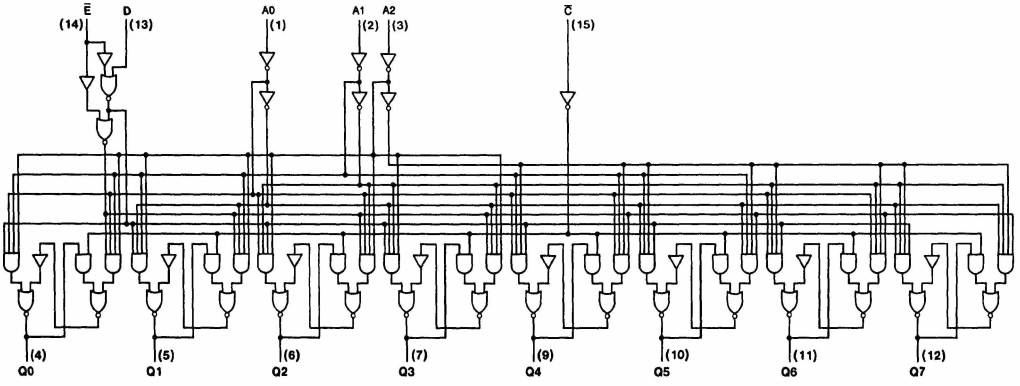

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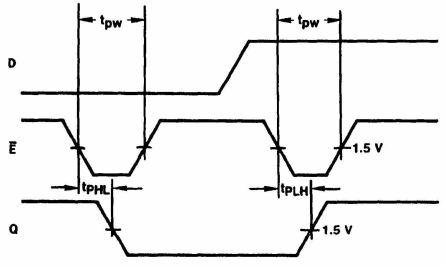
Switching Time Waveforms



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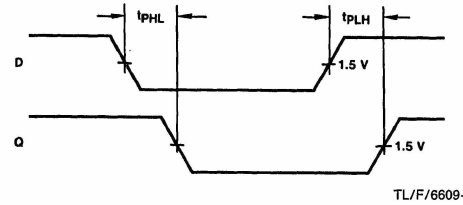
Other Conditions: C = H, A = Stable

Figure 1



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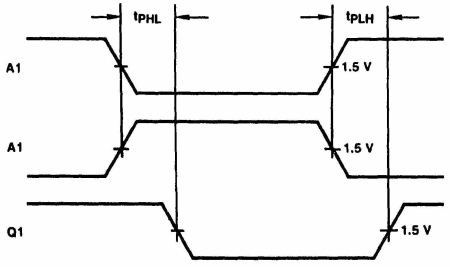
Other Conditions: Ē = L, C̄ = H, A = Stable

Figure 2



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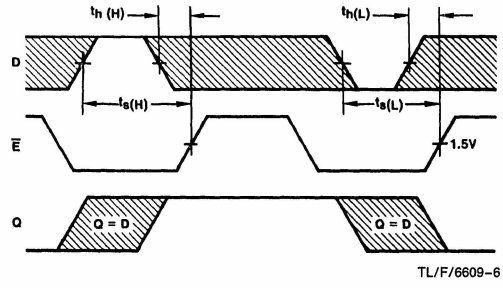
Other Conditions: Ē = L, C̄ = L, D = H

Figure 3



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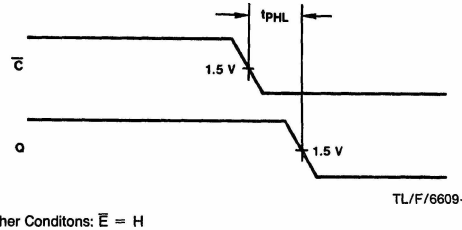
Other Conditions: C = H, A = Stable

Figure 4



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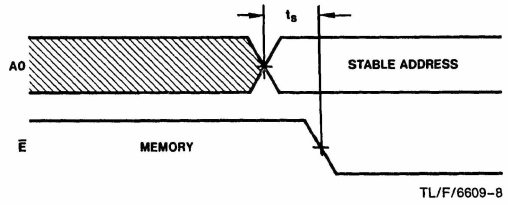
Other Conditons: Ē = H

Figure 5



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Other Conditions: C̄ = H

Figure 6

Note: The shaded areas indicate when the inputs are permitted to change for predictable output performance.