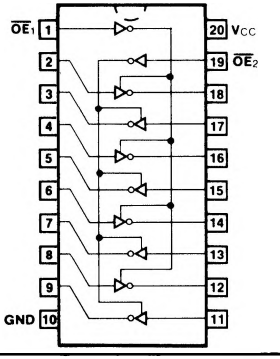
54S/74S240 • 54LS/74LS240
54S/74S241 • 54LS/74LS241
54LS/74LS244

OCTAL BUFFER/LINE DRIVER

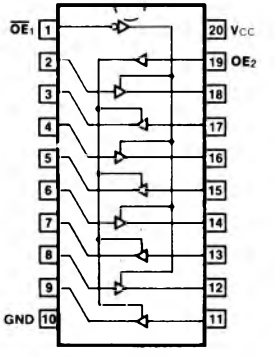
(With 3-State Outputs)

CONNECTION DIAGRAMS

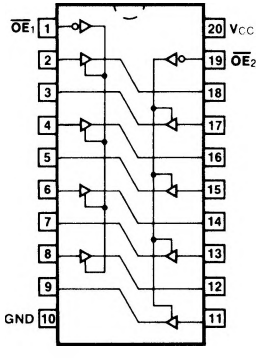
PINOUT A



PINOUT B



PINOUT C



DESCRIPTION — The '240, '241 and '244 are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus oriented transmitters/receivers which provide improved PC board density.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS**
- **3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS**
- **OUTPUTS SINK 24 mA (74LS) OR 40 mA(74S)**
- **15 mA SOURCE CURRENT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V, ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V, ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S240PC, 74LS240PC		9Z
	B	74S241PC, 74LS241PC		
	C	74LS244PC		
Ceramic DIP (D)	A	74S240DC, 74LS240DC	54S240DM, 54LS240DM	4E
	B	74S241DC, 74LS241DC	54S241DM, 54LS241DM	
	C	74LS244DC	54LS244DM	
Flatpak (F)	A	74S240FC, 74LS240FC	54S240FM, 54LS240FM	4F
	B	74S241FC, 74LS241FC	54S241FM, 54LS241FM	
	C	74LS244FC	54LS244FM	

INPUT LOADING/FAN-OUT: See Section 9

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{OE_1}$, $\overline{OE_2}$	3-State Output Enable (Active LOW)	1.25/1.25	0.5/0.25
OE_2	3-State Output Enable (Active HIGH)	1.25/1.25	0.5/0.25
	Inputs	1.25/0.25	0.5/0.125
	Outputs	75/40 (30)	75/15 (7.5)

TRUTH TABLES

'S240, 'LS240

INPUTS			OUTPUT
$\overline{OE_1}$, $\overline{OE_2}$		D	
L		L	H
L		H	L
H		X	Z

'S241, 'LS241

INPUTS			OUTPUT
$\overline{OE_1}$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

'LS244

INPUTS			OUTPUT
$\overline{OE_1}$, $\overline{OE_2}$		D	
L		L	L
L		H	H
H		X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DESCRIPTION				54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage			XM	2.0		2.0		V	I_{OH} = -12 mA, V_{IH} = 2.0 V, V_{IL} = 0.5 V
				XC	2.0		2.0		V	I_{OH} = -15 mA, V_{CC} = Min
				XM	2.4		2.4		V	V_{CC} = Min, V_{IH} = 2.0 V, V_{IL} = Max, I_{OH} = -3.0 mA
				XC	2.4		2.4		V	
				XC	2.7		2.7		V	V_{CC} = Min, V_{IH} = 2.0 V, V_{IL} = Max, I_{OH} = -1.0 mA
V_{OL}	Output LOW Voltage			XM				0.4	V	I_{OL} = 12 mA, V_{CC} = Min
				XC				0.4	V	I_{OL} = 12 mA, V_{CC} = Min
				XC				0.5	V	I_{OL} = 24 mA, V_{CC} = Min
				XM		0.55			V	I_{OL} = 48 mA, V_{CC} = Min
				XC		0.55			V	I_{OL} = 64 mA, V_{CC} = Min
I_{OS}	Output Short Circuit Current				-50	-225	-40	-225	mA	V_{CC} = Max
I_{CC}	Power Supply Current	HIGH	('240)	XM		123		23	mA	V_{CC} = Max
				XC		135		23		
			('241)	XM		147		23		
				XC		160		23		
			('244)	XM				23		
				XC				23		
		LOW	('240)	XM		145		44	mA	V_{CC} = Max
				XC		150		44		
			('241)	XM		170		46		
				XC		180		46		
			('244)	XM				46		
				XC				46		
		OFF	('240)	XM		145		50	mA	V_{CC} = Max
				XC		150		50		
			('241)	XM		170		54		
				XC		180		54		
			('244)	XM				54		
				XC				54		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 50 pF, R_L = 90 Ω		54/74LS C_L = 50 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('240)		7.0 7.0		14 18	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('241)		9.0 9.0		18 18	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('244)				18 18	ns	
t_{PZH} t_{PZL}	Output Enable Time ('S240)		10 15			ns	Figs. 3-3, 3-11, 3-12
t_{PZH} t_{PZL}	Output Enable Time ('LS240, 'LS241, 'S241)		12 15		23 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω ('LS)
t_{PLZ} t_{PHZ}	Output Disable Time		15 9.0		25 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF ('LS)