

# 54/7476

## 54H/74H76

### 54LS/74LS76

#### DUAL JK FLIP-FLOP

(With Separate Sets, Clears and Clocks)

**DESCRIPTION** — The '76 and 'H76 are dual JK master/slave flip-flops with separate Direct Set, Direct Clear and Clock Pulse inputs for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

#### TRUTH TABLE

| INPUTS  |   | OUTPUT      |
|---------|---|-------------|
| @ $t_n$ |   | @ $t_n + 1$ |
| J       | K | Q           |
| L       | L | $Q_n$       |
| L       | H | L           |
| H       | L | H           |
| H       | H | $\bar{Q}_n$ |

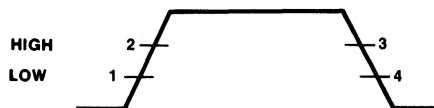
H = HIGH Voltage Level

L = LOW Voltage Level

$t_n$  = Bit time before clock pulse.

$t_n + 1$  = Bit time after clock pulse.

#### CLOCK WAVEFORM



#### Asynchronous Inputs:

LOW input to  $\bar{S}_D$  sets Q to HIGH level

LOW input to  $\bar{C}_D$  sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$

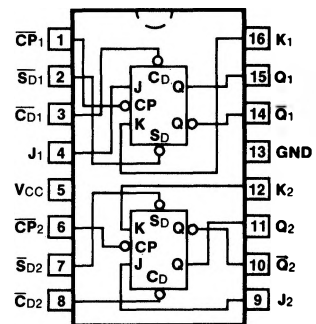
makes both Q and  $\bar{Q}$  HIGH

The 'LS76 is a dual JK, negative edge-triggered flip-flop also offering individual Direct Set, Direct Clear and Clock Pulse inputs. When the Clock Pulse input is HIGH, the JK inputs are enabled and data is accepted. This data will be transferred to the outputs according to the Truth Table on the HIGH-to-LOW clock transitions.

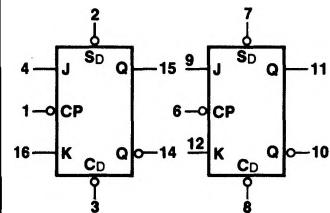
#### ORDERING CODE: See Section 9

| PKGS            | PIN OUT | COMMERCIAL GRADE                                                                       | MILITARY GRADE                                                                             | PKG TYPE |
|-----------------|---------|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|----------|
|                 |         | $V_{CC} = +5.0 \text{ V} \pm 5\%$ ,<br>$T_A = 0^\circ \text{C to } +70^\circ \text{C}$ | $V_{CC} = +5.0 \text{ V} \pm 10\%$ ,<br>$T_A = -55^\circ \text{C to } +125^\circ \text{C}$ |          |
| Plastic DIP (P) | A       | 7476PC, 74H76PC<br>74LS76PC                                                            |                                                                                            | 9B       |
| Ceramic DIP (D) | A       | 7476DC, 74H76DC<br>74LS76DC                                                            | 5476DM, 54H76DM<br>54LS76DM                                                                | 6B       |
| Flatpak (F)     | A       | 7476FC, 74H76FC<br>74LS76FC                                                            | 5476FM, 54H76FM<br>54LS76FM                                                                | 4L       |

#### CONNECTION DIAGRAM PINOUT A



#### LOGIC SYMBOL

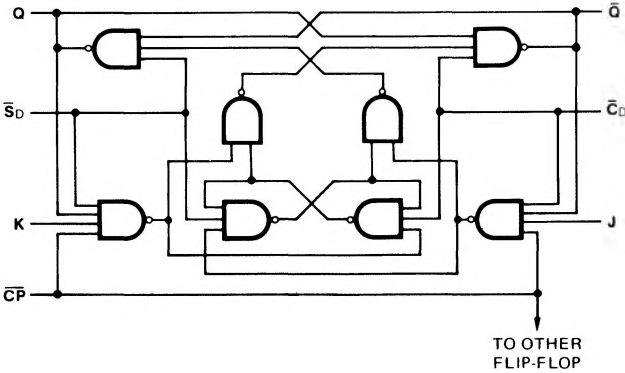


$V_{CC}$  = Pin 5  
GND = Pin 13

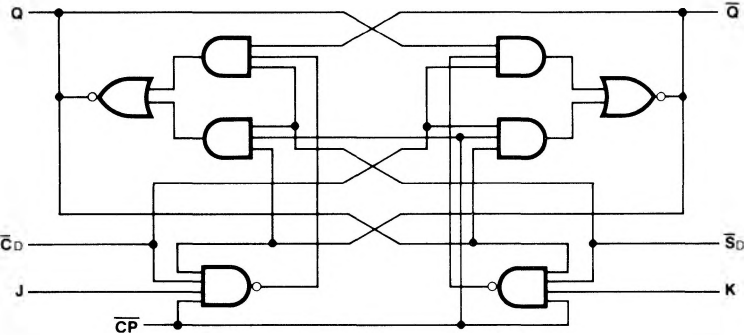
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES                                                                           | DESCRIPTION                              | 54/74 (U.L.)<br>HIGH/LOW | 54/74H (U.L.)<br>HIGH/LOW | 54/74LS (U.L.)<br>HIGH/LOW |
|-------------------------------------------------------------------------------------|------------------------------------------|--------------------------|---------------------------|----------------------------|
| J <sub>1</sub> , J <sub>2</sub> , K <sub>1</sub> , K <sub>2</sub>                   | Data Inputs                              | 1.0/1.0                  | 1.25/1.25                 | 0.5/0.25                   |
| $\overline{\text{CP}}_1$ , $\overline{\text{CP}}_2$                                 | Clock Pulse Inputs (Active Falling Edge) | 2.0/2.0                  | 2.5/2.5                   | 2.0/0.5                    |
| $\overline{\text{CD}}_1$ , $\overline{\text{CD}}_2$                                 | Direct Clear Inputs (Active LOW)         | 2.0/2.0                  | 2.5/2.5                   | 1.5/0.5                    |
| $\overline{\text{SD}}_1$ , $\overline{\text{SD}}_2$                                 | Direct Set Inputs (Active LOW)           | 2.0/2.0                  | 2.5/2.5                   | 1.5/0.5                    |
| Q <sub>1</sub> , $\overline{\text{Q}}_1$ , Q <sub>2</sub> , $\overline{\text{Q}}_2$ | Outputs                                  | 20/10                    | 12.5/12.5                 | 10/5.0<br>(2.5)            |

**LÓGIC DIAGRAMS** (one half shown)  
**'76, 'H76**



**'LS76**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL          | PARAMETER            | 54/74   | 54/74H  | 54/74LS | UNITS | CONDITIONS                                      |
|-----------------|----------------------|---------|---------|---------|-------|-------------------------------------------------|
|                 |                      | Min Max | Min Max | Min Max |       |                                                 |
| I <sub>CC</sub> | Power Supply Current | 40      | 50      | 8.0     | mA    | V <sub>CC</sub> = Max,<br>V <sub>CP</sub> = 0 V |

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL                               | PARAMETER                                                                              | 54/74                                            | 54/74H                                           | 54/74LS                | UNITS | CONDITIONS      |
|--------------------------------------|----------------------------------------------------------------------------------------|--------------------------------------------------|--------------------------------------------------|------------------------|-------|-----------------|
|                                      |                                                                                        | C <sub>L</sub> = 15 pF<br>R <sub>L</sub> = 400 Ω | C <sub>L</sub> = 25 pF<br>R <sub>L</sub> = 280 Ω | C <sub>L</sub> = 15 pF |       |                 |
|                                      |                                                                                        | Min Max                                          | Min Max                                          | Min Max                |       |                 |
| f <sub>max</sub>                     | Maximum Clock Frequency                                                                | 15                                               | 25                                               | 30                     | MHz   | Figs. 3-1, 3-9  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>C <sub>Pn</sub> to Q <sub>n</sub> or $\bar{Q}_n$                  | 25<br>40                                         | 21<br>27                                         | 20<br>30               | ns    | Figs. 3-1, 3-9  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>$\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$ | 25<br>40                                         | 13<br>24                                         | 20<br>30               | ns    | Figs. 3-1, 3-10 |

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

| SYMBOL                                   | PARAMETER                                                             | 54/74    | 54/74H   | 54/74LS    | UNITS | CONDITIONS                                            |
|------------------------------------------|-----------------------------------------------------------------------|----------|----------|------------|-------|-------------------------------------------------------|
|                                          |                                                                       | Min Max  | Min Max  | Min Max    |       |                                                       |
| t <sub>s</sub> (H)                       | Setup Time HIGH<br>J <sub>n</sub> or K <sub>n</sub> to $\bar{C}_{Pn}$ | 0        | 0        | 20         | ns    | Fig. 3-18<br>( '76, 'H76)<br><br>Fig. 3-7<br>( 'LS76) |
| t <sub>h</sub> (H)                       | Hold Time HIGH<br>J <sub>n</sub> or K <sub>n</sub> to $\bar{C}_{Pn}$  | 0        | 0        | 0          | ns    |                                                       |
| t <sub>s</sub> (L)                       | Setup Time LOW<br>J <sub>n</sub> or K <sub>n</sub> to $\bar{C}_{Pn}$  | 0        | 0        | 20         | ns    |                                                       |
| t <sub>h</sub> (L)                       | Hold Time LOW<br>J <sub>n</sub> or K <sub>n</sub> to $\bar{C}_{Pn}$   | 0        | 0        | 0          | ns    |                                                       |
| t <sub>w</sub> (H)<br>t <sub>w</sub> (L) | $\bar{C}_{Pn}$ Pulse Width                                            | 20<br>47 | 12<br>28 | 20<br>13.5 | ns    | Fig. 3-9                                              |
| t <sub>w</sub> (L)                       | $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width LOW                      | 25       | 16       | 25         | ns    | Fig. 3-10                                             |