54ACT818

54ACT818 8-Bit Diagnostic Register

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National Semiconductor

54ACT818
8-Bit Diagnostic Register

General Description

The 'ACT818 is a high-speed, general-purpose pipeline register with an on-board diagnostic register for performing serial diagnostics and/or writable control store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the diagnostic register to operate as a right-shift-only register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with 'ACT818 diagnostic pipeline registers. The loop can be used to scan in a complete test routine starting point (Data, Address, etc.). Then after a specified number of machine cycles it scans out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

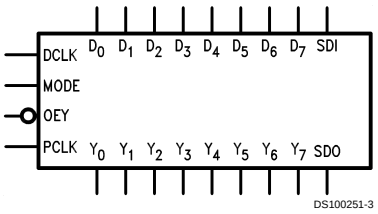
Features

- On-line and off-line system diagnostics
- Swaps the contents of diagnostic register and output register
- Diagnostic register and diagnostic testing
- Cascadable for wide control words as used in microprogramming
- Edge-triggered D registers
- Outputs source/sink 24 mA
- 'ACT818 has TTL-compatible inputs
- 'ACT818 is functionally- and pin-compatible to AMD Am29818 and MMI 74S818
- Standard Microcircuit Drawing (SMD) 5962-9160901

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/serial-parallel converter

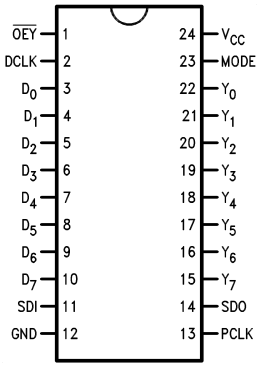
Logic Symbol



DS100251-3

Connection Diagrams

Pin Assignment for DIP and Flatpak



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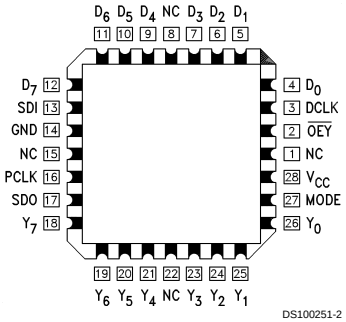
Pin Assignment for LCC



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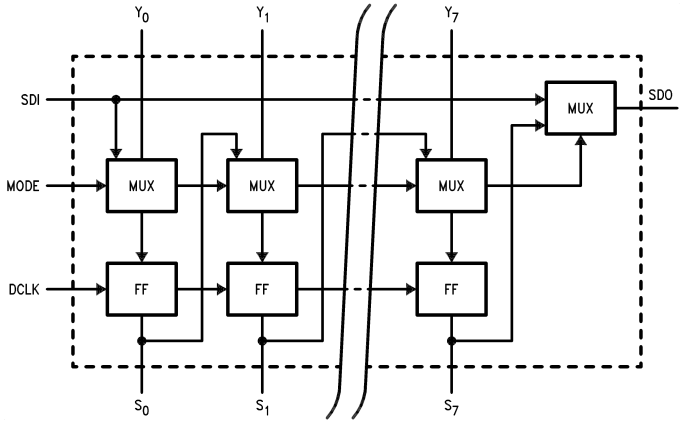
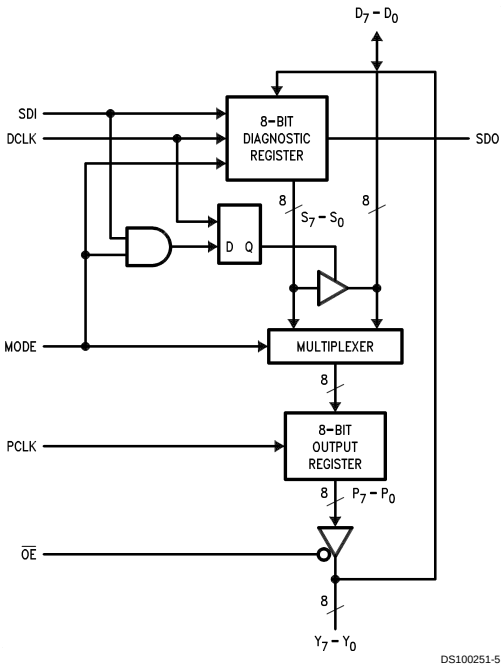
Pin Names	Description
D_0–D_7	Data Inputs
SDI	Serial Data Input
DCLK	Diagnostics Clock
MODE	Control Input
PCLK	Pipeline Register Clock
$\overline{OEY}$	Output Enable Input
SDO	Serial Data Output
Y_0–Y_7	Data Outputs

Diagnostic Register



DS100251-4

Block Diagram



Functional Description

Data transfers into the diagnostic register occur on the LOW-to-HIGH transition of DCLK. Mode and SDI determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. Mode selects whether the data source is the data input or the diagnostic register output. Because of the independence of the clock inputs, data can be shifted in the diagnostic register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously, as long as no setup or hold times are violated. This simultaneous operation is legal.

Function Table

Inputs				Outputs			Operation
SDI	**MODE**	**DCLK**	**PCLK**	**SDO**	**Diagnostic Reg.**	**Pipeline Reg.**	
X	L	N	X	S7	SI<SI − 1, SO<SD_I	NA	Serial Shift; D_7–D_0 Disabled
X	L	X	N	S7	NA	PI<DI	Normal Load Pipeline Register
L	H	N	X	L	SI<YI	NA	Load Diagnostic Register from Y; DI Disabled
X	H	X	N	SDI	NA	PI<SI	Load Pipeline Register from Diagnostic Register
H	H	N	X	H	Hold	NA	Hold Diagnostic Register; DI Enabled

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
N = LOW-to-HIGH Clock Transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACT	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Note 2: All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8		V_{OUT} = 0.1V or V_{CC} − 0.1V
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_{IN} = V_{CC}
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±1.0	µA	$\overline{OE}$ = V_{IH} V_{OUT} = 0V, V_{CC}
I_{CC}	Maximum Quiescent Supply Current	5.5	160	µA	V_{IN} = V_{CC} or GND
I_{CCT}	Maximum Additional I_{CC}/Input	5.5	1.6	mA	V_{IN} = V_{CC} − 2.1V V_{CC} = 5.5V
V_{OH}	Minimum HIGH				(Note 2) V_{IN} = V_{IL} or V_{IH}
	Level Output Voltage, Y_0–Y_7 Outputs	4.5 5.5	3.70 4.70	V V	I_{OH} = −24 mA I_{OH} =−24 mA
	Minimum HIGH Level Output Voltage, D_0–D_7, SDO Outputs	4.5 5.5	3.70 4.70	V V	I_{OH} = −8 mA I_{OH} = −8 mA
V_{OL}	Maximum LOW				(Note 2) V_{IN} = V_{IL} or V_{IH}
	Level Output Voltage, Y_0–Y_7 Outputs	4.5 5.5	0.50 0.50	V V	I_{OL} = 24 mA I_{OL} = 24 mA
	Maximum LOW Level Output Voltage, D_0–D_7, SDO Outputs	4.5 5.5	0.50 0.50	V V	I_{OL} = 8 mA I_{OL} = 8 mA

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{OLD}	Minimum Dynamic Output Current, Y_0–Y_7 Outputs	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Minimum Dynamic Output Current, Y_0–Y_7 Outputs	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{OLD}	Minimum Dynamic Output Current, D_0–D_7, SDO Outputs (Note 4)	5.5	32	mA	V_{OLD} = 1.65V Max
I_{OHD}	Minimum Dynamic Output Current, D_0–D_7, SDO Outputs (Note 4)	5.5	−32	mA	V_{OHD} = 3.85V Min

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Test load 50 pF, 500Ω to ground.

Note 5: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 6)	54ACT T_A = −55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
t_{PHL}	Propagation Delay PCLK to Y	5.0	2.5	10.0	ns	
t_{PLH}	Propagation Delay PCLK to Y	5.0	2.5	10.0	ns	
t_{PHL}	Propagation Delay MODE to SDO	5.0	3.5	12.0	ns	
t_{PLH}	Propagation Delay MODE to SDO	5.0	3.5	13.5	ns	
t_{PHL}	Propagation Delay SDI to SDO	5.0	3.0	11.5	ns	
t_{PLH}	Propagation Delay SDI to SDO	5.0	3.0	12.0	ns	
t_{PHL}	Propagation Delay DCLK to SDO	5.0	3.5	14.0	ns	
t_{PLH}	Propagation Delay DCLK to SDO	5.0	3.5	15.5	ns	
t_{PZL}	Output Enable Time $\overline{OEY}$ to Y_n	5.0	2.5	12.0	ns	
t_{PLZ}	Output Disable Time $\overline{OEY}$ to Y_n	5.0	1.5	10.0	ns	
t_{PZL}	Output Enable Time DCLK to D_n	5.0	3.0	14.0	ns	

AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V) (Note 6)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
t_{PLZ}	Output Disable Time DCLK to D_n	5.0	1.5	12.0	ns	
t_{PZH}	Output Enable Time $\overline{OEY}$ to Y_n	5.0	2.5	11.0	ns	
t_{PHZ}	Output Disable Time $\overline{OEY}$ to Y_n	5.0	2.0	12.0	ns	
t_{PZH}	Output Enable Time DCLK to D_n	5.0	3.0	13.5	ns	
t_{PHZ}	Output Disable Time DCLK to D_n	5.0	2.0	13.5	ns	

Note 6: Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 8)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_s	Setup Time D to PCLK	5.0	6.0	ns	
t_h	Hold Time D to PCLK	5.0	1.0	ns	
t_s	Setup Time MODE to PCLK	5.0	6.0	ns	
t_h	Hold Time MODE to PCLK	5.0	0.0	ns	
t_s	Setup Time Y to DCLK	5.0	2.5	ns	
t_h	Hold Time Y to DCLK	5.0	1.5	ns	
t_s	Setup Time MODE to DCLK	5.0	4.5	ns	
t_h	Hold Time MODE to DCLK	5.0	1.0	ns	
t_s	Setup Time SDI to DCLK	5.0	4.5	ns	
t_h	Hold Time SDI to DCLK	5.0	1.0	ns	
t_s	Setup Time DCLK to PCLK	5.0	11.5	ns	
t_s	Setup Time PCLK to DCLK	5.0	12.5	ns	
t_w	Pulse Width	5.0	3.5	ns	

AC Operating Requirements (Continued)

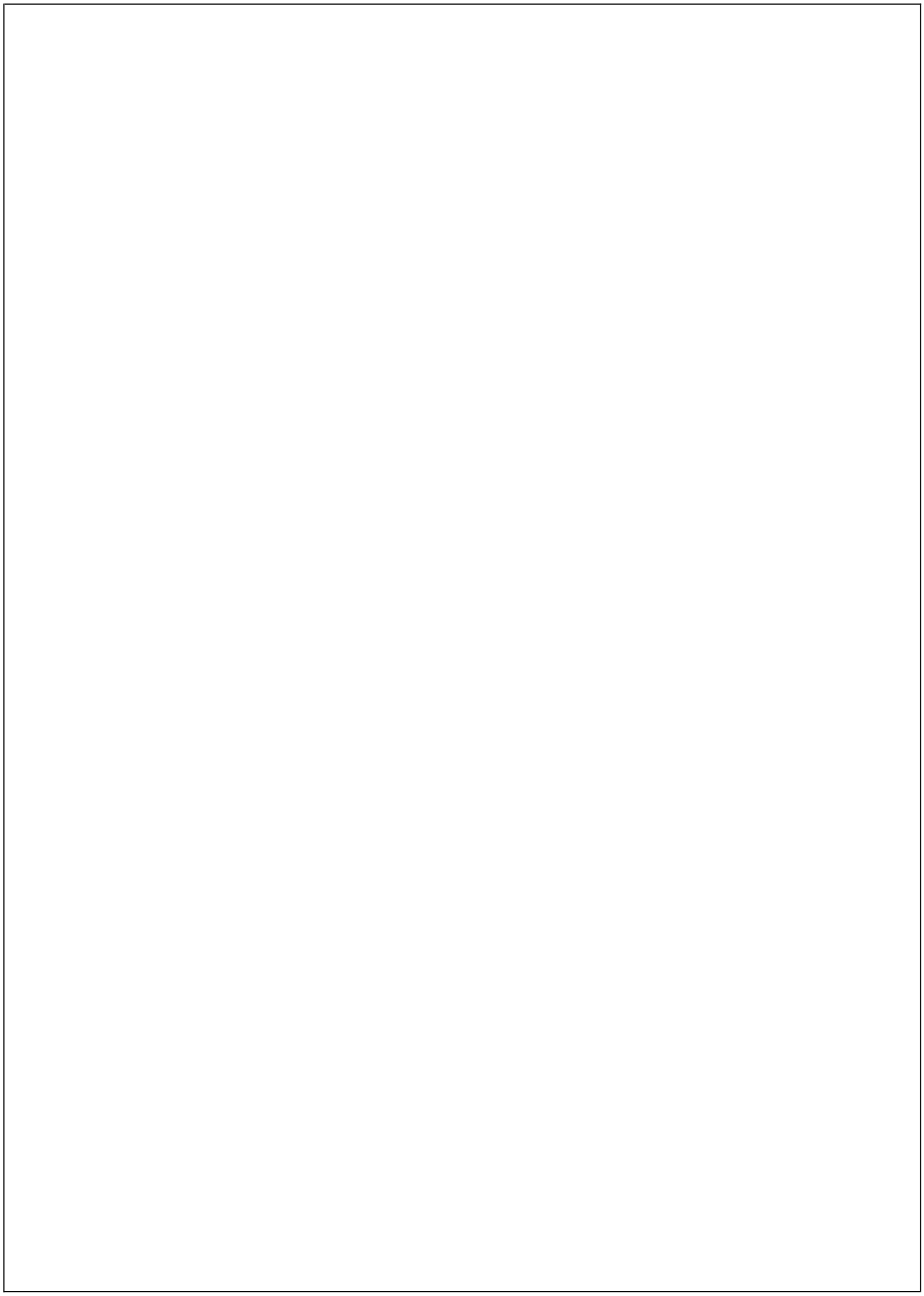
Symbol	Parameter	V_{CC} (V) (Note 8)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
	PCLK HIGH or LOW				
t_w	Pulse Width DCLK HIGH or LOW	5.0	3.0	ns	

Note 7: Test load 50 pF, 500Ω to ground.

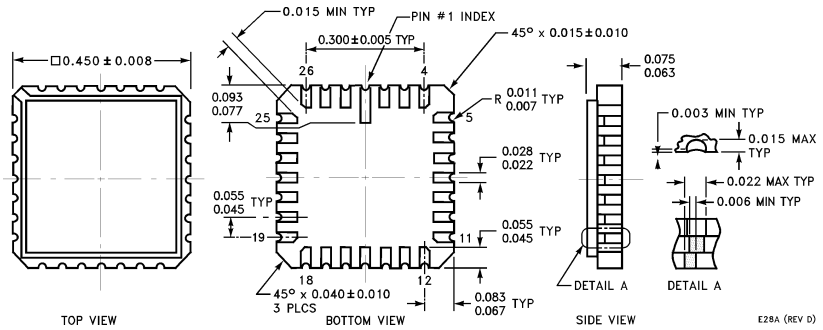
Note 8: Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

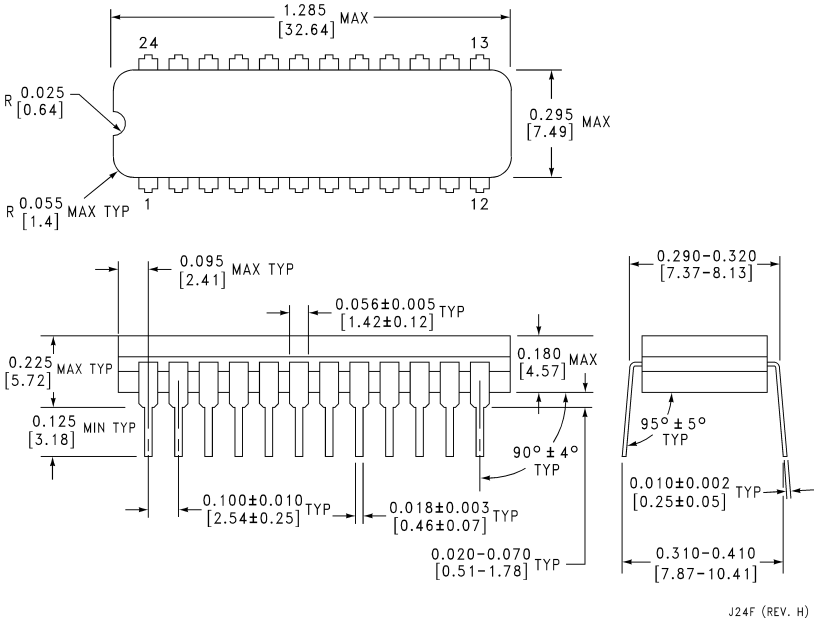
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	20	pF	V_{CC} = 5.0V



Physical Dimensions inches (millimeters) unless otherwise noted

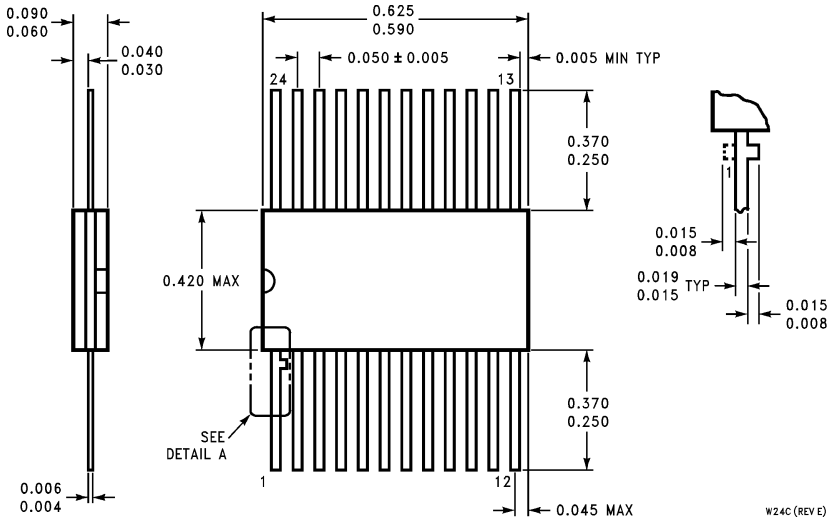


28 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



24 Lead Slim (0.300" wide) Ceramic Dual-in-Line Package (D)
NS Package Number J24F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24 Lead Ceramic Cerpack
NS Package Number W24C

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