DESCRIPTION

The 2102A is a high speed static random access memory element using n-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. A low standby power version (2102AL) is also available, and has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.

A separate chip enable ($\overline{CE}$) lead allows easy selction of an individual package when outputs are OR-tied.

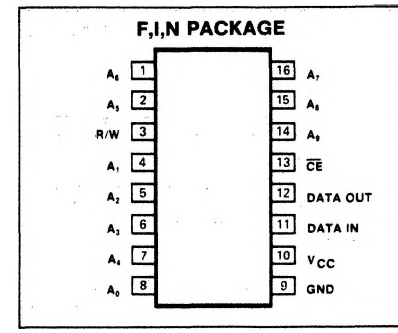
The 2102A is fabricated with n-channel silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or p-channel silicon gate technology.

FEATURES

- **Single 5V supply voltage**
- **Fully TTL compatible**
- **Standby power mode (2102AL)**
- **Tri-state output**
- **OR-tie capability**
- **All inputs protected against static charge**
- **Low cost packaging**

PIN CONFIGURATION

F,I,N PACKAGE



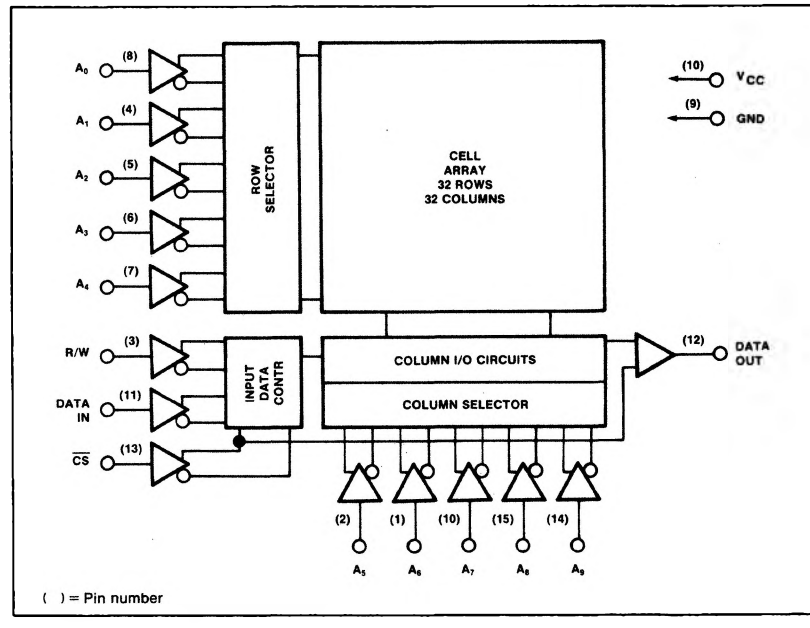
PIN DESIGNATION

PIN NO.	SYMBOL	FUNCTION	TYPE
11	D_{IN}	Data input	
1,2,4-8,14,16	A_0-A_9	Address inputs	
3	R/W	Read/write input	
13	$\overline{CE}$	Chip enable	
12	D_{OUT}	Data output	
10	V_{CC}	Power (5V)	
9	GND	Ground	

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	High Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	-10 to 80	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	2102A/2102A-4/ 2102AL/2102AL-4			2102A-2/ 2102AL-2			2102A-6			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage											V
V_{IL}	Low		-0.5		0.8	-0.5		0.8	-0.5		0.65	
V_{IH}	High		2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	
	Output voltage											V
V_{OL}	Low	I_{OL} = 2.1mA			0.4			0.4			0.45	
V_{OH}	High	I_{OH} = -100μA	2.4			2.4			2.2			
I_{LI}	Input load current	V_{IN} = 0 to 5.25V		1	10		1	10		1	10	μA
	Output leakage current	$\overline{CE}$ = 2.0V										μA
I_{LOH}		$V_{OUT} = V_{OH}$		1	5		1	5		1	5	
I_{LOL}		V_{OUT} = 0.4V		-1	-10		-1	-10		-1	-10	
I_{CC}	Supply current[3]	Data out open, $T_A = 0°C$		33			45	65		33	55	mA
	Capacitance[4]											pF
C_{IN}	Input (All pins)	V_{IN} = 0V		3	5		3	5		3	5	
C_{OUT}	Output	V_{OUT} = 0V		7	10		7	10		7	10	

STANDBY CHARACTERISTICS $T_A = 0°C$ to $70°C$

PARAMETER		TEST CONDITIONS	2102AL, 2102AL-4			2102AL-2			UNIT
			Min	Typ[5]	Max	Min	Typ[5]	Max	
V_{PD}	V_{CC} in standby		1.5			1.5			V
V_{CES}	$\overline{CE}$ bias in standby[6]	2.0V ≤ V_{PD} ≤ V_{CC} max	2.0			2.0			V
		1.5V ≤ V_{PD} < 2.0V	V_{PD}			V_{PD}			
	Standby current								mA
I_{PD1}		All inputs = V_{PD1} = 1.5V		15	23		20	28	
I_{PD2}		All inputs = V_{PD2} = 2.0V		20	30		25	38	
t_{CP}	Chip deselect to standby time		0			0			ns
t_R	Standby recovery time[7]		t_{RC}			t_{RC}			ns

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise noted,
Input pulse levels = 0.8V to 2.0V, Input rise and fall times = 10ns,
Timing measurement reference level inputs = 1.5V
Output = 0.8V and 2.0V, Output load = 1 TTL gate and C_L = 100pF

	PARAMETER	TO	FROM	2102A-2, 2102AL-2			2102A, 2102AL			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_{RC}	Read cycle			250			350			ns
t_A	Access time					250			350	ns
t_{CO}		Output time	Chip enable			130			180	ns
	Previous read data valid with respect to									ns
t_{OH1}	Address			40			40			
t_{OH2}	Chip enable			0			0			
	WRITE CYCLE									
t_{WC}	Write cycle			250			350			ns
t_{WP}	Write pulse width			180			250			ns
t_{WR}	Write recovery time			0			0			ns
	Setup and hold time									ns
t_{AW}	Setup time	Write	Address	20			20			
t_{DW}	Setup time	R/W	Data	180			250			
t_{DH}	Hold time	Output	Data	0			0			
t_{CW}	Setup time	Data	R/W	180			250			

	PARAMETER	TO	FROM	2102A-4, 2102AL-4			2102A-6			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_{RC}	Read cycle			450			650			ns
t_A	Access time					450			650	ns
t_{CO}		Output time	Chip enable			230			400	ns
	Previous read data valid with respect to									ns
t_{OH1}	Address			40			50			
t_{OH2}	Chip enable			0			0			
	WRITE CYCLE									
t_{WC}	Write cycle			450			650			ns
t_{WP}	Write pulse width			300			400			ns
t_{WR}	Write recovery time			0			50			ns
	Setup and hold time									ns
t_{AW}	Setup time	Write	Address	20			200			
t_{DW}	Setup time	R/W	Data	300			450			
t_{DH}	Hold time	Output	Data	0			20			
t_{CW}	Setup time	Data	R/W	300			550			

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.
4. This parameter is periodically sampled and is not 100% tested.
5. Typical values are for T_A = 25°C.
6. Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V (V_{CC} max) and 2.0V, then $\overline{CE}$ must be held at 2.0V min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the 2.
7. $t_R = t_{RC}$ (read cycle time).

VOLTAGE WAVEFORMS