DESCRIPTION

The Signetics 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T25 Sense Amp, and 3207 Clock Driver.

FEATURES

- **LOW POWER DISSIPATION – DISSIPATES POWER PRIMARILY ON SELECTED CHIPS**
- **ACCESS TIME – 300 nsec.**
- **CYCLE TIME – 580 nsec.**
- **REFRESH PERIOD – 2 MILLISECONDS FOR 0-70°C AMBIENT**
- **OR-TIE CAPABILITY**
- **SIMPLE MEMORY EXPANSION WITH CHIP ENABLE**
- **FULLY DECODED – ON-CHIP ADDRESS DECODE**
- **INPUTS PROTECTED – ALL INPUTS HAVE PROTECTION AGAINST STATIC CHARGE.**
- **LOW COST PACKAGING –18 PIN SILICONE AND 18 PIN CERAMIC DUAL IN-LINE**

APPLICATIONS

CORE MEMORY REPLACEMENT
BUFFER STORES
MAIN MEMORY

PROCESS TECHNOLOGY

The use of Signetics' unique silicon gate low threshold process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

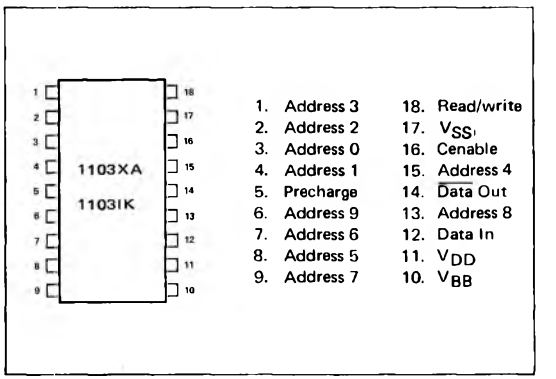
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric

SILICONE PACKAGING (Cont'd)

material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

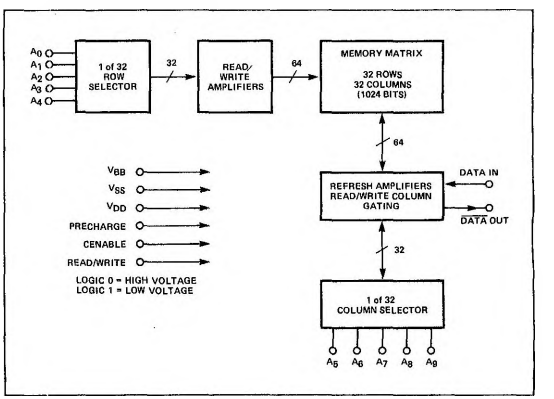
PIN CONFIGURATION (Top View)



PART IDENTIFICATION TABLE

TYPE	PACKAGE	OP. TEMP. RANGE
1103XA	18-Pin DIP Silicone	0-70°C
1103IK	18-Pin DIP Ceramic	0-70°C

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS(10)

Operating Ambient Temperature	0°C to 70°C	Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.0W
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V		

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS}(1) = 16V ± 5%, ($V_{BB} - V_{SS}$)(6) = 3V to 4V, V_{DD} = 0V unless otherwise specified (Note 9).

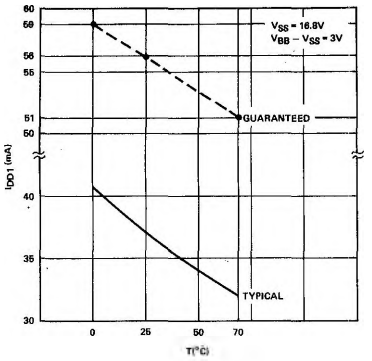
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All input pins)			1	μA	V_{IN} = 0V, T_A = 25°C
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0V, T_A = 25°C
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}(2)	Supply Current During t_{PC}		37	56	mA	All Addresses = 0V Precharge = 0V Cenable = V_{SS}; T_A = 25°C
I_{DD2}(2)	Supply Current During t_{OV}		38	59	mA	All Addresses = 0V Precharge = 0V Cenable = 0V; T_A = 25°C
I_{DD3}(2)	Supply Current During t_{POV}		5.5	11	mA	Precharge = V_{SS} Cenable = 0V; T_A = 25°C
I_{DD4}(2)	Supply Current During t_{CP}		3	4	mA	Precharge = V_{SS} Cenable = V_{SS}; T_A = 25°C
I_{DD}(5)AV	Average Supply Current		17	25	mA	Cycle Time = 580 ns; Precharge Width = 190 ns; T_A = 25°C
V_{IL1}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.2	V	T_A = 0°C
V_{IL2}(7)	Input Low Voltage (All Address & Data-in Lines)	V_{SS}−17		V_{SS}−14.5	V	T_A = 70°C
V_{IL3}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−14.7	V	T_A = 0°C
V_{IL4}(7,8)	Input Low Voltage (Precharge Cenable & Read/Write Inputs)	V_{SS}−17		V_{SS}−15.0	V	T_A = 70°C
V_{IH1}(7)	Input High Voltage (All Inputs)	V_{SS}−1		V_{SS}+1	V	T_A = 0°C
V_{IH2}(7)	Input High Voltage (All Inputs)	V_{SS}−0.7		V_{SS}+1	V	T_A = 70°C
I_{OH1}	Output High Current	600	900	4000	μA	T_A = 25°C
I_{OH2}	Output High Current	500	800	4000	μA	T_A = 70°C
I_{OL}	Output Low Current	See Note 3				- R_{LOAD} = 100Ω(4)
V_{OH1}	Output High Voltage	60	90	400	mV	T_A = 25°C
V_{OH2}	Output High Voltage	50	80	400	mV	T_A = 70°C
V_{OL}	Output Low Voltage	See Note 3				

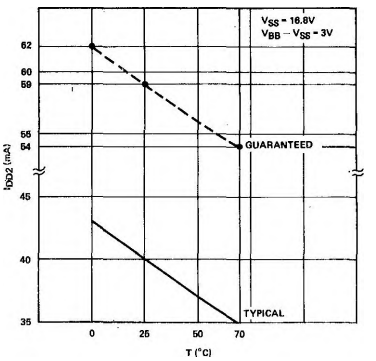
NOTES:

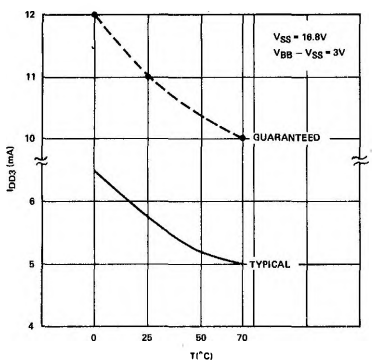
1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.
5. This parameter is periodically sampled and is not 100% tested.
6. ($V_{BB} - V_{SS}$) supply should be applied at or before V_{SS}.
7. The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value between 0°C and 70°C can be calculated using a straight-line relationship.
8. The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to V_{SS}−14.2 @ 0°C and V_{SS}−14.5 @ 70°C (same values as those specified for the address and data-in lines) with a 40 ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

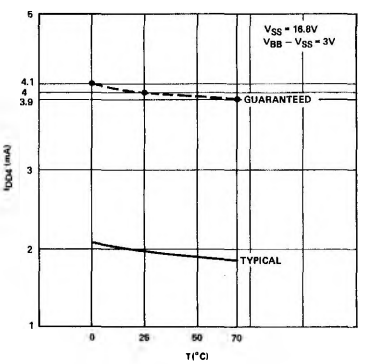
CHARACTERISTIC CURVES

SUPPLY CURRENT VS TEMPERATURE

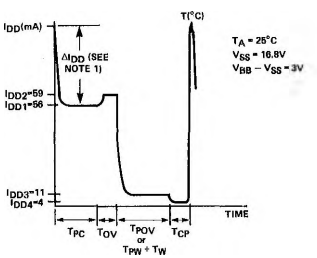








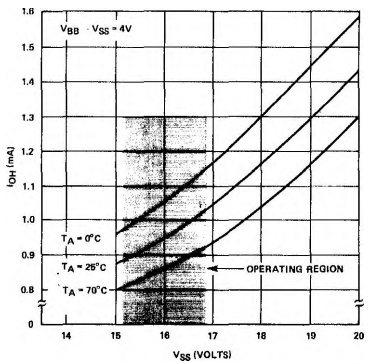
I_{DD} VS TIME

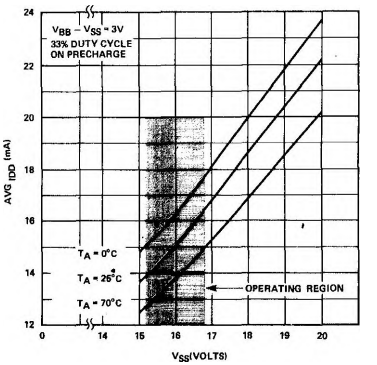


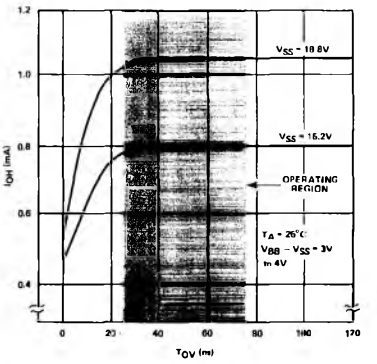
NOTES:

1. ΔI_{DD} is due to charging of internal device node capacitance at precharge.
2. These values are taken from a single pulse measurement.

CHARACTERISTIC CURVES (Cont'd)







AC CHARACTERISTICS $T_A = 25°C$, $V_{SS} = 16 \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	Time Between Refresh			2	ms	
t_{AC}(1)	Address to Cenable Set Up Time	115			ns	
t_{CA}	Cenable to Address Hold Time	20			ns	
t_{PC}(1)	Precharge to Cenable Delay	125			ns	
t_{OVL}	Precharge & Cenable Overlap, Low	25		75	ns	
t_{CP}	Cenable to Precharge Delay	85			ns	
t_{OVH}	Precharge & Cenable Overlap, High			140	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC}(1)	Read Cycle	480			ns	
t_{POV}	Precharge to End of Cenable	165		500	ns	
t_{PO}	End of Precharge to Output Delay			120	ns	t_T = 20 ns
t_{ACC1}(1)	Address to Output Access	300			ns	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$ — C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{ACC2}(1)	Precharge to Output Access	310			ns	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$

AC CHARACTERISTICS (Cont'd)

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}(1)	Write Cycle	580			ns	t_T = 20 ns
t_{RWC}(1)	Read/Write Cycle	580			ns	
t_{PW}	Precharge to Read/Write Delay	165		500	ns	
t_{WP}	Read/Write Pulse Width	50			ns	
t_W	Read/Write Set Up Time	80			ns	
t_{DW}	Data Set Up Time	105			ns	
t_{DH}	Data Hold Time	10			ns	
t_{PO}	End of Precharge to Output Delay			120	ns	C_{LOAD} = 100 pF R_{LOAD} = 100Ω V_{REF} = 40 mV
t_P	Time to Next Precharge	0			ns	
t_{CW}	Read/Write Hold Time			10	ns	

CAPACITANCE (note 2)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C_{AD}	Address Capacitance		5	7	pF	$V_{IN} = V_{SS}$
C_{PR}	Precharge Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance		15	18	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance		11	15	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance		4	5	pF	Cenable = 0V $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance		2	4	pF	Cenable = V_{SS} $V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance		2	3	pF	V_{OUT} = 0V

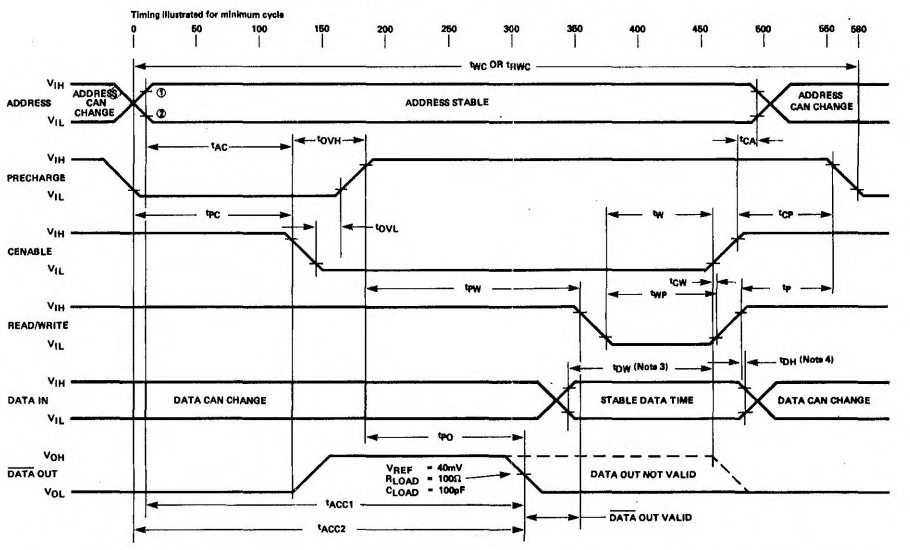
f = 1 MHz
All Unused Pins are at A.C. Ground

(1) These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS} − 14.2V @ 0°C and V_{SS}−14.5V @ 70°C as defined on page 2.

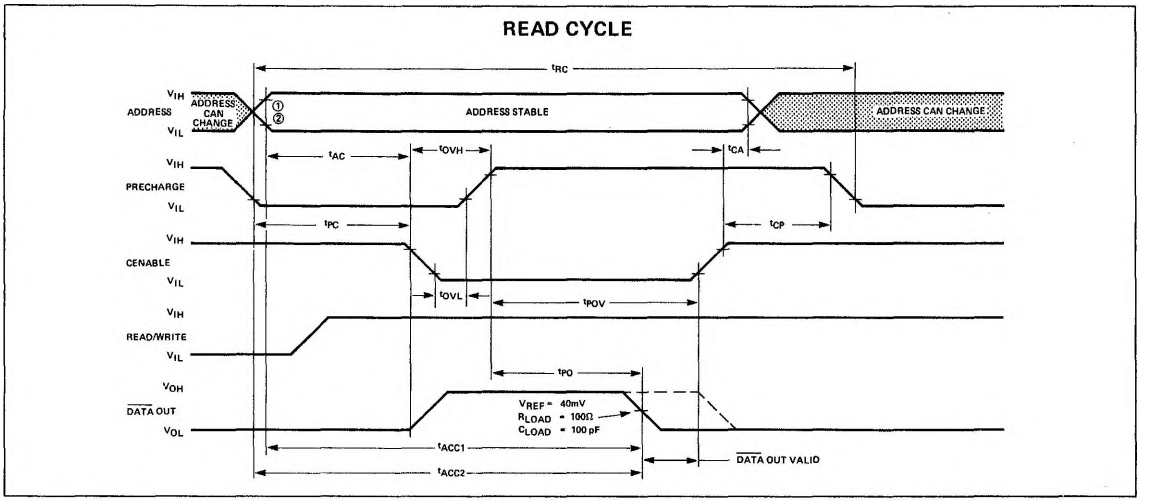
(2) This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic packages only.

TIMING DIAGRAM

WRITE CYCLE OR READ/WRITE CYCLE



TIMING DIAGRAM (Cont'd)



NOTES:

① $V_{DD} + 2V$ ② $V_{SS} - 2V$ — t_T is defined as the transitions between these two points.

3 t_{DW} is referenced to point ② of the rising edge of cenable or read/write whichever occurs first.

4 t_{DH} is referenced to point ① of the rising edge of cenable or read/write whichever occurs first.

CIRCUIT SCHEMATIC